UNIT - V

7 Bipolar Junction Transistor

7.1 : Introduction

Q.1 What is transistor ? ☞[JNTU : Part A]

Ans. : • Transistor is a three terminal device : Base, emitter and collector, can be operated in three configurations common base, common emitter and common collector.

• According to configuration it can be used for voltage as well as current amplification.

Q.2 Explain the word transistor. ☞[JNTU : Part A]

Ans. : • The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance. This concept of transfer of resistance has given the name TRANSfer-resISTOR (TRANSISTOR).

Q.3 State the two types of transistors. ☞[JNTU : Part A]

Ans. : There are two types of transistors : **Unipolar junction transistor** and **Bipolar junction transistor.**

Q.4 Why transistor is also called bipolar junction transistor ? ☞[JNTU : Part A]

Ans. : The current conduction in bipolar transistor is because of both the types of charge carriers, holes and electrons. Hence this is called **Bipolar junction transistor.**

Q.5 What are the types of BJT ? ☞[JNTU : Part A]

Ans. : 1. n-p-n type 2. p-n-p type

Q.6 State the advantages of transistor. ☞[JNTU : Part A]

Ans. : The key advantages that have allowed transistors to replace vacuum tubes in most applications are :

1. Very small size and weight, reducing equipment size
2. Low operating voltages
3. Lower costs
4. Low power consumption
5. Higher efficiency
6. Very long life
7. Very low sensitivity to mechanical shock and vibration.

Q.7 State the applications of trasistor. ☞[JNTU : Part A]

Ans. : Applications of transistor :

1. Transistor can be used as an amplifier and switch.
2. Transistor can be used as an amplifier. It is used as a current and voltage amplifier.
3. As a switch, transistor is used in SMPS (Switch Mode Power Supply) and digital circuits.
4. Transistors are used in oscillator circuits and feedback amplifiers.

7.2 Construction of BJT

Q.8 Explain the construction of npn and pnp transistor. ☞[JNTU : Part B, June - 17, Marks 5]

OR What is an NPN transistor ? ☞[JNTU : Part A, June - 17, Marks 2]

Ans. : • When a transistor is formed by sandwiching a single p-region between two n-regions, as shown in the Fig. Q.8.1 (a), it is an n-p-n type transistor. The p-n-p type transistor has a single n-region between two p-regions, as shown in Fig. Q.8.1 (b).

• The middle region of each transistor type is called the **base** of the transistor. This region is very thin and lightly doped.

• The process by which impurities are added to a pure semiconductor is called **doping.**

• The remaining two regions are called **emitter** and **collector.**

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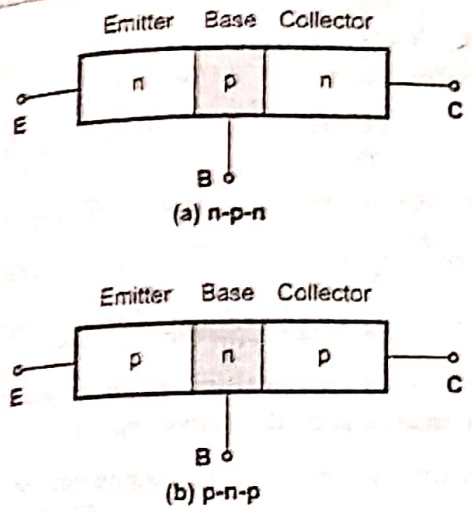

Fig. Q.8.1 Bipolar transistor construction

- The emitter and collector are **heavily** doped. But the doping level in emitter is slightly greater than that of collector.
- The collector region-area is slightly more than that of emitter.

Q.9 Draw the symbols of pnp and npn transistors.

[JNTU : Part A, April-18, Marks 2]

Ans. : • Fig. Q.9.1 (a) and (b) shows the symbols of npn and pnp transistors. Arrow head on a transistor symbol indicates the conventional current which is opposite to the direction of electron current in emitter.

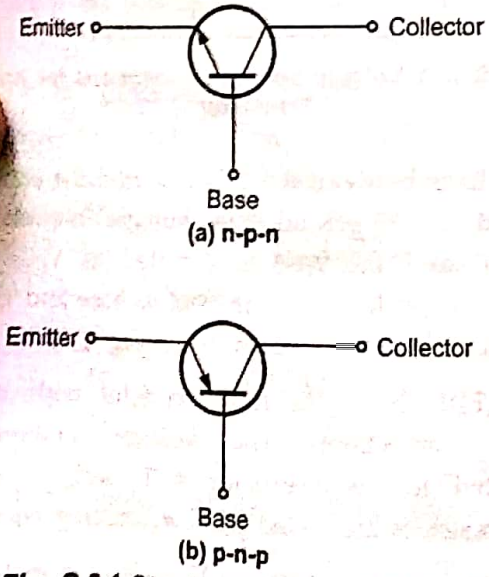

Fig. Q.9.1 Standard transistor symbols

Q.10 State the two junctions in the transistor.

[JNTU : Part A]

Ans. : • A transistor has two p-n junctions.

- One junction is between the emitter and the base and is called the **emitter-base junction** or simply the **emitter junction** J_E.
- The other junction is between the base and the collector and is called **collector-base junction** or simply **collector junction** J_C.

7.3 Principle of Operation

Q.11 Explain the working principle of npn transistor.

[JNTU : Part B, June - 17, Marks 7]

Ans. : • The base to emitter junction is forward biased by the d.c. source V_{EE}. Thus, the width of depletion region at this junction is small. The collector to base junction is reverse biased and hence width of depletion region at this junction is large, shown in Fig. Q.11.1 (Fig. Q.11.1 shows conventional currents).

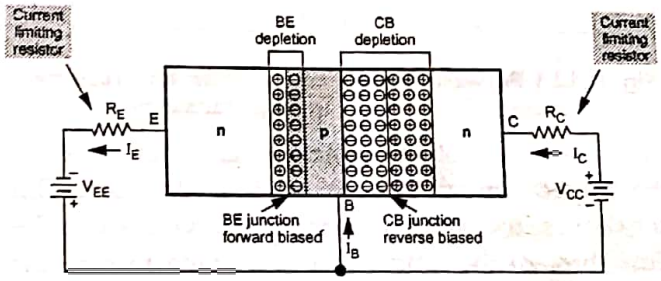

Fig. Q.11.1 Forward biased EB junction and reverse biased CB junction in npn transistor

- The forward biased EB junction causes the electrons in the n-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the p-type base, they tend to combine with holes in p-region (base).
- Due to light doping, very few of the electrons injected into the base from the emitter recombine with holes to constitute base current, I_B and the remaining large number of electrons cross the base region and move through the collector region to the positive terminal of the external d.c. source. This constitutes collector current I_C. Thus the electron flow constitutes the dominant current in an npn transistor.
- Since, the most of the electrons from emitter flow in the collector circuit and very few combine with holes in the base. Thus, the collector current is larger than the base current.

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- The emitter current is summation of base current and collector current.

$$I_E = I_B + I_C$$

Q.12 Explain the working principle of pnp transistor.

☞[JNTU : Part B]

Ans. : • The pnp transistor has its bias voltages V_{EE} and V_{CC} reversed from those in the npn transistor, shown in Fig. Q.12.1 (Fig. Q.12.1 shows conventional currents). This is necessary to forward-bias the emitter-base junction and reverse-bias the collector base junction in pnp transistor.

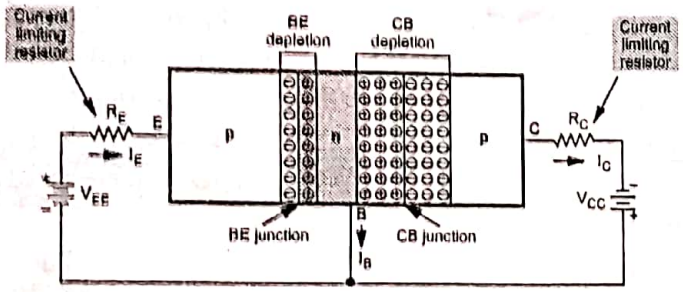

Fig. Q.12.1 Forward biased EB junction and reverse biased CB junction in pnp transistor

- The forward biased EB junction causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes flow through the n-type base, they tend to combine with electrons in n-region (base). As the base is very thin and lightly doped, very few of the holes injected into the base from the emitter recombine with electrons to constitute base current, I_B.
- The remaining large number of holes cross the depletion region and move through the collector region to the negative terminal of the external dc source. This constitutes collector current I_C. Thus the hole flow constitutes the dominant current in an pnp transistor.
- Like npn transistor, in pnp transistor the emitter current is summation of base current and collector current.

$$I_E = I_B + I_C$$

Q.13 State the operating regions of BJT.

☞[Part A]

Ans. : • Depending upon external bias voltage polarities used, the transistor works in one of the three regions : 1) **Active region** 2) **Cut-off region** and 3) **Saturation region.**

Region	Emitter-base junction	Collector-base junction	Application
Active	Forward biased	Reverse biased	Amplifier
Cut-off	Reverse biased	Reverse biased	Off-Switch
Saturation	Forward biased	Forward biased	On-Switch

Table Q.13.1 Operating regions

In order to operate transistor as an amplifier, it is necessary to bias it in the active region.

Q.14 Explain various voltage components of BJT.

☞[JNTU : Part B]

Ans. : • Fig. Q.14.1 shows the terminal voltages and its polarities for an npn transistor. The voltage between base and emitter is denoted as V_{BE}. For V_{BE}, base is positive than emitter because for npn transistor, the base is biased positive with respect to the emitter.

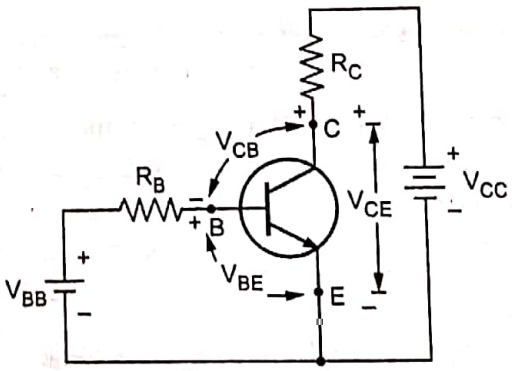

Fig. Q.14.1 Voltage source connections for npn transistor

- The voltage between the collector and the emitter is denoted as V_{CE} and the voltage between the collector and the base is denoted as V_{CB}. Since collector is positive with respect to base and emitter the polarities are as shown in the Fig. Q.14.1.
- Fig. Q.14.1 shows the npn transistor with voltage source connections. The voltage sources are connected to the transistor with series resistors. These resistors are called **current limiting resistors.**
- The base supply voltage V_{BB} is connected via resistor R_B, and the collector supply voltage, V_{CC} is connected via resistor R_C.
- The negative terminals of both the supply voltage are connected to emitter terminal of the transistor.

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To make CB junction reverse biased, the supply voltage V_{CC} is always much larger than supply voltage V_{BB}.

pnp Transistor

The Fig. Q.14.2 shows the terminal voltages and its polarities for a pnp transistor. For a pnp transistor, the base is biased negative with respect to the emitter, and the collector is made more negative than the base.

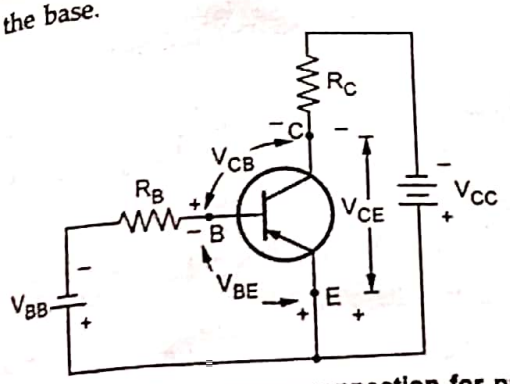

Fig. Q.14.2 Voltage source connection for pnp transistor

- Fig. Q.14.2 shows the pnp transistor with voltage source connections. Like npn transistor voltage sources are connected with series resistors. The source voltage positive terminals are connected at the emitter with V_{CC} larger than V_{BB} to keep collector-base junction reverse biased.

Q.15 State the junction voltages of BJT. [JNTU : Part A]

Ans. : • In different conditions such as active, saturation and cutoff there are different junction voltages. The junction voltages for a typical npn transistor at 25 °C are given in the Table Q.15.1.

Type	$V_{CE\,sat}$	$V_{BE\,sat}$	$V_{BE\,active}$	$V_{BE\,cutin}$	$V_{BE\,cutoff}$
Si	0.2	0.8	0.7	0.5	0.0
Ge	0.1	0.3	0.2	0.1	– 0.1

Table Q.15.1 Typical npn transistor junction voltages at 25 °C

- The entries in the table are appropriate for an npn transistor. For pnp transistor the signs of all entries should be reversed.

Q.16 Explain the various current components of the transistor. [JNTU : Part B]

Ans. : • The directions of conventional currents in an npn transistor are as shown in Fig. Q.16.1 (a) and Fig. Q.16.1 (c) and those for a pnp are shown in Fig. Q.16.1 (b) and Q.16.1 (d). Figures show the conventional currents using the schematic symbols of npn and pnp transistors, respectively.

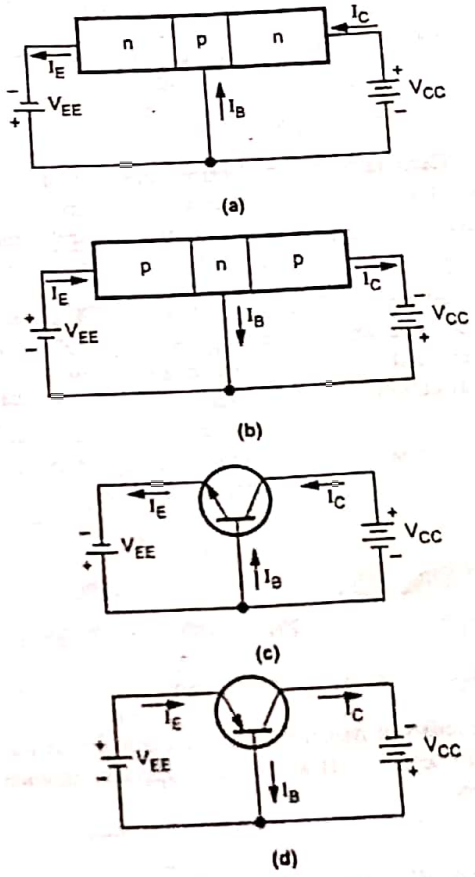

Fig. Q.16.1 Transistor conventional current directions

- It can be noticed that the arrow at the emitter of the transistor's symbol points in the direction of conventional current.
- Let us consider pnp transistor. The current flowing into the emitter terminal is referred to as the emitter current and identified as I_E. The currents flowing out of the collector and base terminals are referred to as collector current and base current, respectively. The collector current is identified as I_C and base current as I_B.

For both npn and pnp transistors.

$$I_E = I_B + I_C$$

Refer Fig. Q.16.1.

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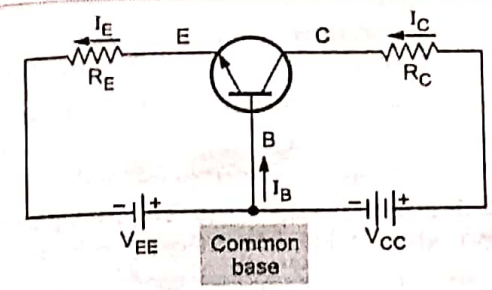
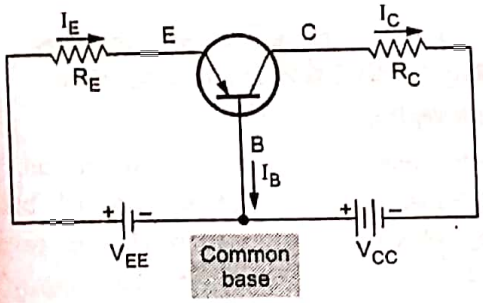


(a) npn



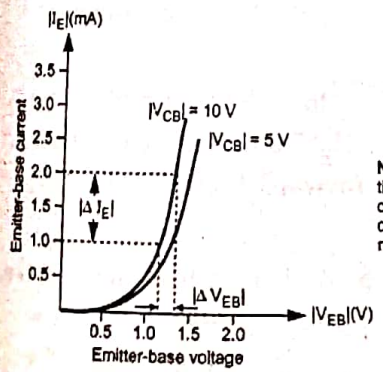
(b) pnp

Fig. Q.20.1 Common base configuration

- Here, base of the transistor is common to both input and output circuits and hence the name common base configuration.

Q.21 Draw and explain the input characteristics of CB configuration. ☞[JNTU : Part B]

Ans. : • It is the curve between input voltage V_{EB} (emitter-base voltage) and input current I_E (emitter current) at constant collector-base voltage V_{CB}. The emitter current is taken along Y-axis and emitter base voltage along X-axis. Fig. Q.21.1 shows the input characteristics of a typical transistor in common-base configuration.



Note : While plotting input characteristics the magnitudes of voltage and current are considered. Practically the voltage and current polarities are opposite for pnp and npn transistors

Fig. Q.21.1 Input characteristics of transistor in CB configuration

- From this characteristics we can observe the following important points :

1. The input resistance is a ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}).
   It is given by
   $$r_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$$
2. After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for germanium), the emitter current (I_E) increases rapidly with small increase in emitter-base voltage (V_{EB}). Thus, the input resistance is very small.
3. It can be observed that there is slight increase in emitter current (I_E) with increase in V_{CB}. This is due to change in the width of the depletion region in the base region under the reverse biased condition.

Q.22 Define $I_{C(INJ)}$ and I_{CBO}. ☞[JNTU : Part A]

Ans. : In common base configuration, the collector current I_C is given by,

$$I_C = I_{C(INJ)} + I_{CBO}$$

$I_{C(INJ)}$: It is an injected collector current due to number of electrons crossing the collector base junction.

I_{CBO} : It is the reverse saturation current flowing due to the minority carrier between collector and base when the emitter is open. I_{CBO} is negligible as compared to $I_{C(INJ)}$ and therefore we have

$$I_C \approx I_{C(INJ)}$$

However, when emitter is open

$$I_C = I_{CBO}$$

I_{CBO} → Emitter open
→ Collector to base leakage current

Key Point : The reverse saturation current, I_{CBO}, is temperature sensitive and it doubles for every 10 °C rise in temperature.

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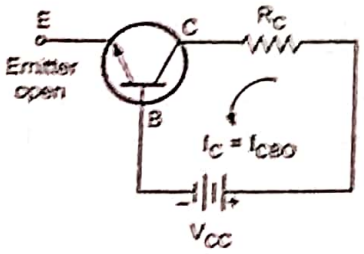

Fig. Q.22.1 CB configuration with base open

Q.23 Define current amplification factor or current gain (α_{dc}). [JNTU : Part A]

Ans. : It is defined as the ratio of the collector current resulting from carrier injection to the total emitter current.

$$\therefore \quad \alpha_{dc} = \alpha \approx \frac{I_{C(INJ)}}{I_E} = \frac{I_C}{I_E}$$

$\because I_{CBO}$ is negligibly small

Since $I_C < I_E$ the value of α_{dc} is always less than unity. It ranges from 0.95 to 0.995 depending on the thickness of the base region; larger the thickness of the base, smaller is the value of α_{dc}.

Q.24 What is early effect? How can it account for the CB input characteristics ? [JNTU : Part B]

Ans. : • When reverse bias voltage V_{CB} increases, the width of depletion region also increases, which reduces the electrical base width. This effect is called as 'Early effect' or 'Base width modulation'.

• This decrease in base width has two consequences.

1. There is less chance for recombination within the base region. Hence the transport factor β^*, and also α, increase with an increase in the magnitude of the collector junction voltage.
2. The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the junction increases. This increases emitter current slighily. Refer Fig. Q.24.1.

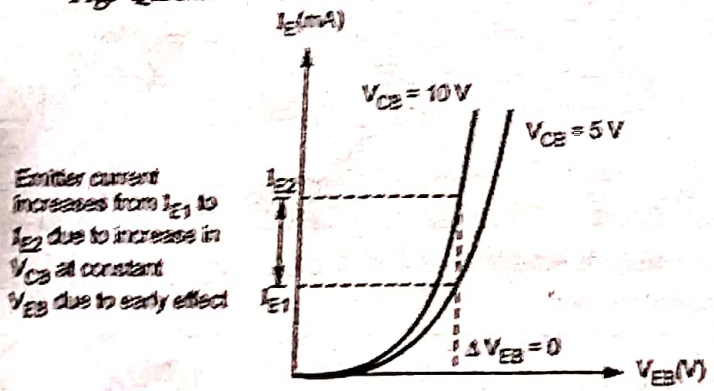

Fig. Q.24.1

Q.25 Draw and explain the output characteristics of CB configuration. [JNTU : Part B]

Ans. : • It is the curve between collector current I_C and collector base voltage V_{CB} at constant emitter current I_E. The collector current is taken along Y-axis and collector-base voltage magnitude along X-axis. Fig. Q.25.1 shows the output characteristics of a typical transistor in common base configuration.

From this characteristics we observe following points :

1. The output characteristics has three basic regions : **Active, cut-off and saturation.**
2. **Active region :**
   - For the operation in the active region, the emitter-base junction (J_E) is **forward biased** while collector base junction (J_C) is **reverse biased.**
   - In this region, collector current I_C is approximately equal to the emitter current (I_E) and transistor works as an amplifier.
   - In the active region, the collector current is essentially almost constant.
   - The Dynamic output resistance is the ratio of change in collector base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current (I_E). It is given by

$$R_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{Constant}}$$

   - The collector current I_C is almost independent on collector-base voltage V_{CB} and the transistor can be said to work as constant-current source. This provides very high dynamic output resistance.
3. **Saturation region** : In this region, the emitter-base junction (J_E) and collector base junction (J_C) both are **forward biased.** Here, the I_C is independent of I_B.
4. **Cut-off region** : The region below the curve $I_E = 0$ is known as cut-off region, where the collector current is nearly zero and the collector-base (J_C) and emitter-base (J_E) junctions of a transistor are **reverse biased.**

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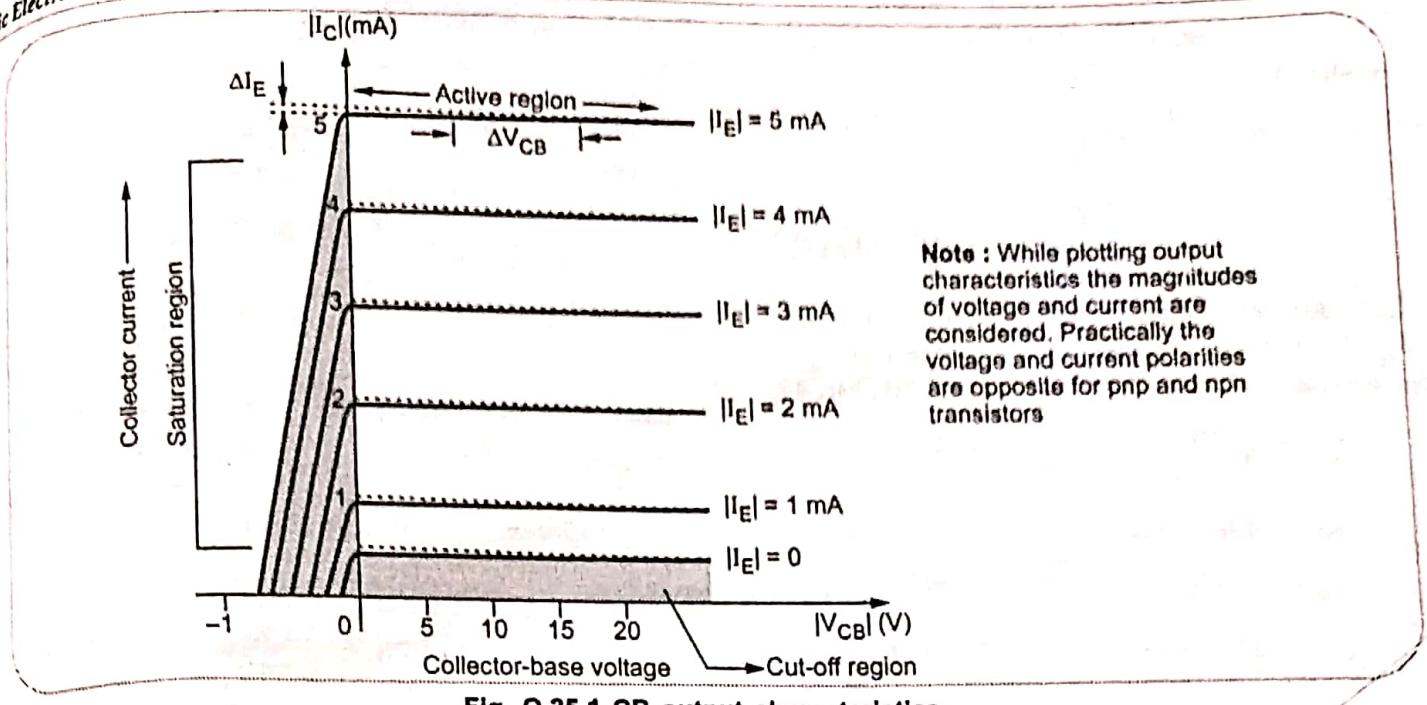
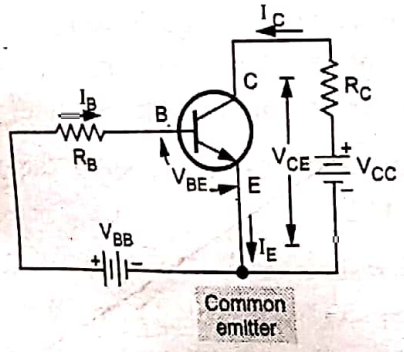


Fig. Q.25.1 CB output characteristics

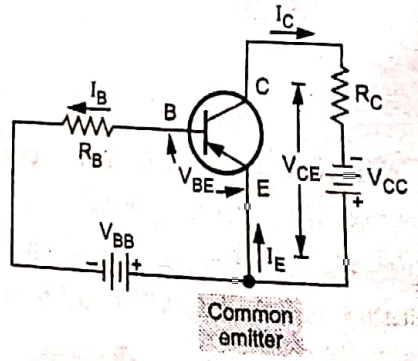
26 Draw the circuit configuration of CE nnection. ☞ **[JNTU : Part A, June - 17, Marks 2]**

ns. : • In this configuration input is applied tween base and emitter, and output is taken from llector and emitter. Here, emitter of the transistor is mmon to both, input and output circuits, and hence e name common emitter configuration.

Common emitter configurations for both npn and pnp transistors are shown in Fig. Q.26.1 (a) and Q.26.1 (b), respectively.



(a) npn



(b) pnp

Fig. Q.26.1 Common emitter configurations

Q.27 Define β_{dc}. ☞ **[JNTU : Part A]**

Ans. : • The β_{dc} is the ratio of output current I_C and input current I_B in common emitter configuration. It is **common emitter amplification factor** or **current gain.**

• It is given by,

$$\beta_{dc} = \frac{I_C}{I_B}$$

Q.28 Derive the relationship between α_{dc} and β_{dc}. ☞ **[JNTU : Part B]**

Ans. :

$$\beta = \frac{I_C}{I_B}$$

We have, $I_E = I_C + I_B$ i.e. $I_B = I_E - I_C$

$$\beta = \frac{I_C}{I_E - I_C}$$

$\because$ $I_B = I_E - I_C$

Dividing the numerator and denominator of R.H.S. of above equation by I_E, we get,

$$\beta = \frac{I_C/I_E}{I_E/I_E - I_C/I_E}$$

$\therefore$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \qquad \because \alpha = \frac{I_C}{I_E}$$

We know that, $\alpha = \frac{I_C}{I_E}$ and $I_E = I_B + I_C$

$$\alpha = \frac{I_C}{I_B + I_C}$$

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Dividing the numerator and denominator of R.H.S. of above equation by I_B, we get,

$$\alpha = \frac{I_C/I_B}{I_B/I_B + I_C/I_B}$$

$$\therefore \quad \alpha = \frac{\beta}{1+\beta} \qquad \because \beta = \frac{I_C}{I_B}$$

Q.29 Calculate the values of I_C and I_E for a BJT with $\alpha_{dc} = 0.97$ and $I_B = 50\ \mu A$. Determine β_{dc} for the device. [JNTU : Part B]

Ans. : $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.97}{1-0.97} = 32.33$

$I_C = \beta I_B = 32.33 \times 50\ \mu A = 1.6165\ mA$

$I_E = I_B + I_C$

$= 50\ \mu A + 1.6165\ mA = 1.6665\ mA$

Q.30 Define reverse leakage current (I_{CEO}) in CE configuration. [JNTU : Part B]

Ans. : In CE configuration,

$$I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CBO} \qquad \ldots(1)$$

The terms $(1 + \beta_{dc}) I_{CBO}$ in equation (1) is denoted as I_{CEO} and is the reverse saturation current for the CE configuration.

$$\therefore \quad I_C = \beta_{dc} I_B + I_{CEO} \qquad \because (1+\beta_{dc}) I_{CBO} = I_{CEO}$$

Q.31 For a transistor in common emitter configuration, the reverse leakage current is 21 μA, whereas when the same transistor is connected in common base configuration, it reduces to 1.1 μA. Calculate values of α_{dc} and β_{dc} of the transistor. [JNTU : Part B]

Ans. : Given : $I_{CBO} = 1.1\ \mu A$, $I_{CEO} = 21\ \mu A$

$$I_{CEO} = (1 + \beta_{dc})\ I_{CBO}$$

$$\therefore \quad 1 + \beta_{dc} = \frac{I_{CEO}}{I_{CBO}} = \frac{21\ \mu A}{1.1\ \mu A} = 19.09$$

$$\therefore \quad \beta_{dc} = 18.09$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{18.09}{1+18.09} = 0.9476$$

Q.32 Calculate the α_{dc} and β_{dc} for the given transistor for which $I_C = 5$ mA, $I_B = 50\ \mu A$ and $I_{CO} = 1\ \mu A$.

Ans. : $I_C = 5\ mA$, $I_B = 50\ \mu A$, $I_{CO} = I_{CBO} = 1\ \mu A$

$$I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CBO}$$

$$\therefore \quad 5\times10^{-3} = \beta_{dc} \times 50\times10^{-6} + (1+\beta_{dc}) \times 1\times10^{-6}$$

$$\therefore \quad 5\times10^{-3} - 1\times10^{-6} = 51\times10^{-6}\ \beta_{dc}$$

$$\therefore \quad \beta_{dc} = \frac{4.999\times10^{-3}}{51\times10^{-6}} = 98$$

$$\therefore \quad \alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{98}{1+98} = 0.9899$$

Q.33 The BJT circuit has $I_C = 10$ mA and $\alpha = 0.98$. Determine the value of β and I_E. [JNTU : Part A]

Ans. : Given : $I_C = 10$ mA and $\alpha = 0.98$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$I_E = \frac{(1+\beta) I_C}{\beta} = 10.2\ mA$$

Q.34 Draw and explain the input characteristics of transistor in CE mode. [JNTU : Part B]

Ans. : • The input voltage in the CE configuration is the base-emitter voltage and the output voltage is the collector-emitter voltage. The input current is I_B and the output current is I_C.

• Input characteristics is the curve between input voltage V_{BE} (base-emitter voltage) and input current I_B (base current) at constant collector-emitter voltage, V_{CE}. The base current is taken along Y-axis and base emitter voltage V_{BE} is taken along X-axis. Fig. Q.34.1 shows the input characteristics of a typical transistor in common-emitter configuration.

From this characteristics we observe the following important points :

1. The input resistance is the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector emitter voltage V_{CE}. It is given by,

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{Constant}}$$

2. After the cut-in voltage, the base current (I_B) increases rapidly with small increase in base-emitter voltage (V_{BE}). Thus the dynamic input resistance is small in CE configuration.
3. For a fixed value of V_{BE}, I_B decreases as V_{CE} is increased.

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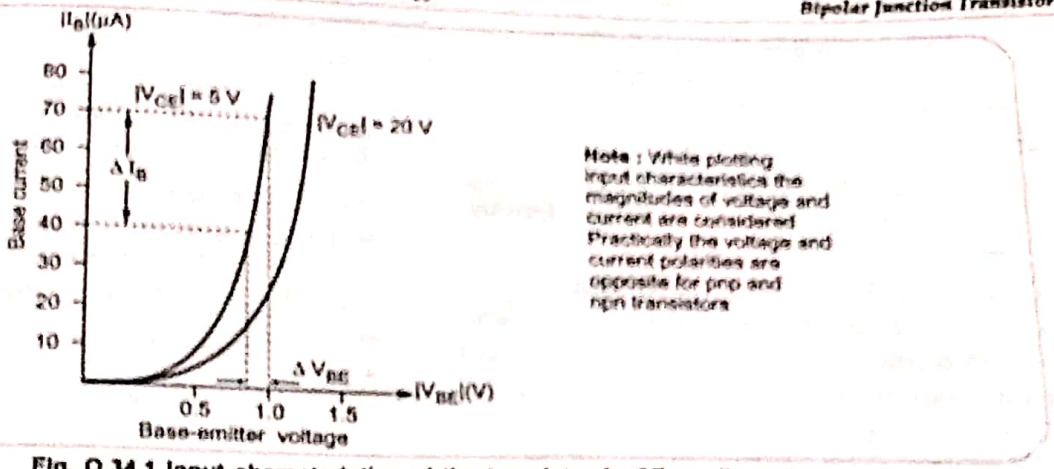

Fig. Q.34.1 Input characteristics of the transistor in CE configuration

Q.35 With a neat diagram explain the output characteristics of npn transistor in CE configuration. **[JNTU : Part B]**

Ans. : 1. This characteristics shows the relation between the collector current I_C and collector voltage V_{CE} for various fixed values of I_B. This characteristics is often called collector characteristics. A typical family of output characteristics for an n-p-n transistor in CE configuration is shown in Fig. Q.35.1.

2. The value of β_{dc} of the transistor can be found at any point on the characteristics by taking the ratio I_C to I_B at that point, i.e. $\beta_{dc} = I_C / I_B$. This is known as D.C. beta for the transistor.

3. From the output characteristics, we can see that change in collector-emitter voltage (ΔV_{CE}) causes the little change in the collector current (ΔI_C) for constant base current I_B. Thus the output dynamic resistance is high in CE configuration.

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{Constant OR } \Delta I_B = 0}$$

- The output characteristics of common emitter configuration consists of three regions : **Active, Saturation and Cut-off.**

Active Region :

- For the operation in the active region, the emitter-base junction (J_E) is **forward biased** while collector base junction (J_C) is **reverse biased.**

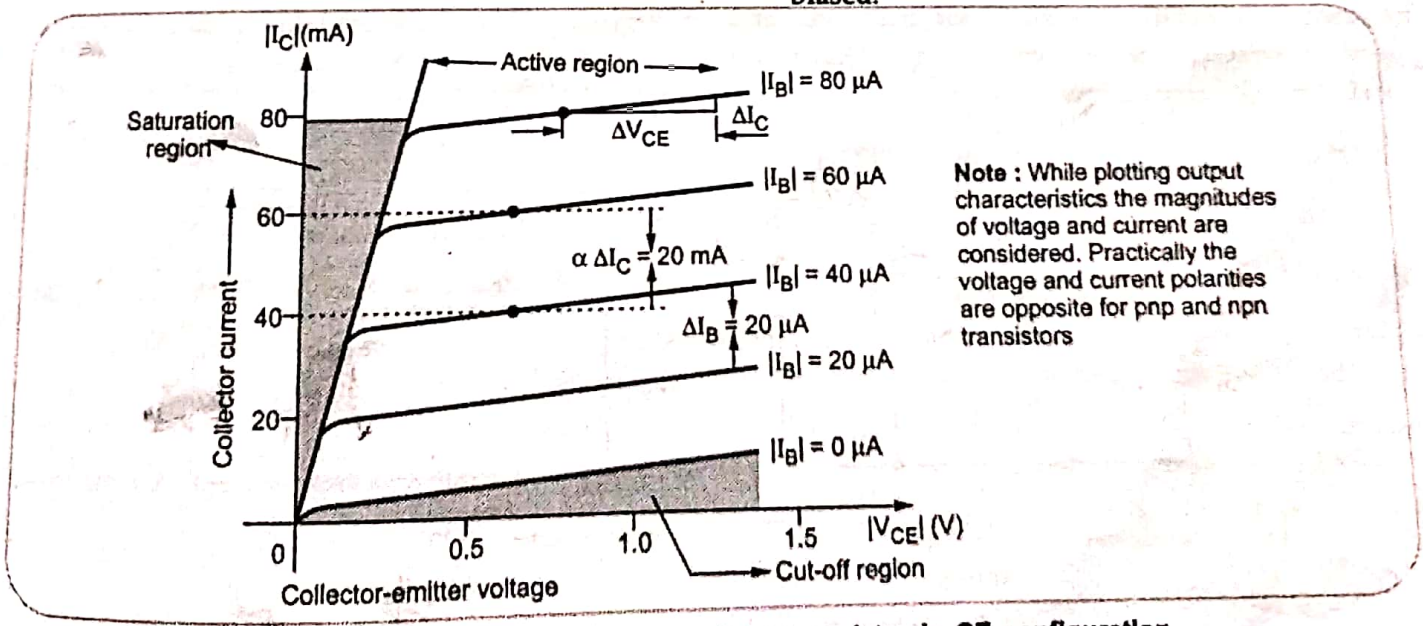

Fig. Q.35.1 Output characteristics of the transistor in CE configuration

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- The collector current rise more sharply with increasing V_{CE} in the linear region of output characteristics of CB transistor.

Saturation region :

- In this region, the emitter-base junction (J_E) and collector base junction (J_C) both are forward biased.
- The saturation value of V_{CE}, designated $V_{CE(sat)}$, usually ranges between 0.1 V to 0.3 V.

Cut-off region :

- The region below $I_B = 0$ is the cut-off region of operation for the transistor. In this region, both the junctions of the transistor are reverse biased.

To identify the operating region of transistor we can observe certain conditions. These are :

For saturation : $I_B > \frac{I_C}{\beta_{dc}}$ For cut-off : $I_B = 0$

For active region : $V_{CE} > V_{CE(sat)}$

Q.36 Draw the neat circuit configuration of CC. [JNTU : Part A]

Ans. : • The Fig. Q.36.1 shows the common collector configuration. In this configuration, input is applied between base and collector and output is taken from emitter and collector.

- Here, collector of the transistor is common to both input and output circuits and hence the name common collector configuration.
- Common collector connections for both npn and pnp transistors are shown in Fig. Q.36.1 (a) and Q.36.1 (b), respectively.
- Here, the output at the emitter follows the input at the base and hence this configuration is also known as emitter follower configuration.

Q.37 Sketch and explain the input characteristics of transistor in CC configuration. [JNTU : Part B]

Ans. : • The input characteristics of CC configuration is a graph of input current I_B (base current) versus input voltage V_{CB} (collector base voltage) at constant V_{CE}. The base current is taken along Y-axis and collector base voltage V_{CB} is taken along X-axis.

- Fig. Q.37.1 shows the input characteristics of a typical transistor in common-collector configuration.

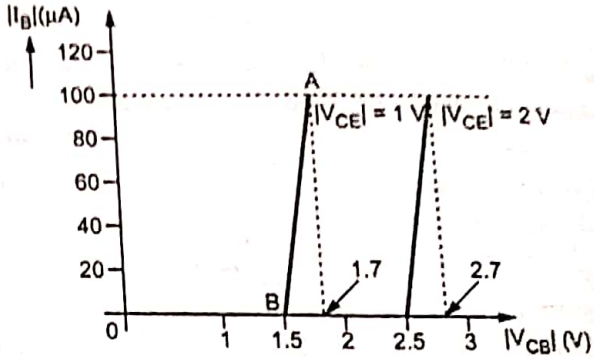

Fig. Q.37.1 Input characteristics of transistor in CC configuration

- The common collector input characteristics are quite different from either common base or common emitter input characteristics.
- This difference is due to the fact that the input voltage V_{CB} is largely determined by the level of collector to emitter voltage V_{CE}.

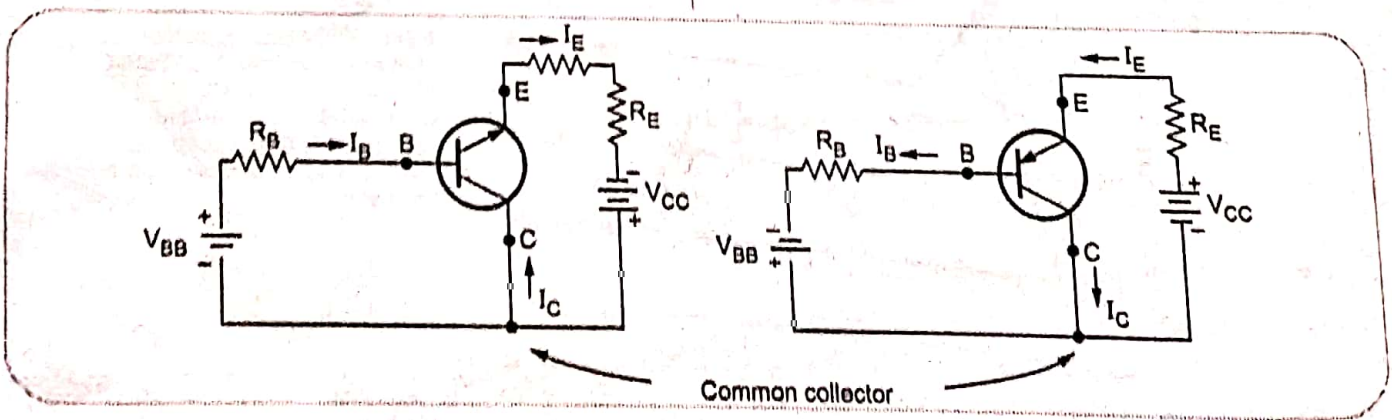

Fig. Q.36.1 Common collector configurations

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- Looking at Fig. Q.37.1 we can write,

$$V_{CE} = V_{CB} - V_{BE}$$

or

$$V_{CB} = V_{CE} + V_{BE}$$

- In CC configuration input junction is BC and it is reversed biased so input resistance in CC configuration is very high.

Q.38 Sketch and explain the output characteristics of transistor in CC configuration. ☞[JNTU : Part B]

Ans. : • It is the curve between emitter current I_E and collector to emitter voltage V_{CE} at constant base current I_B. The emitter current is taken along Y-axis and collector to emitter voltage along X-axis.

• Fig. Q.38.1 shows the output characteristics of a typical transistor in common collector configuration.

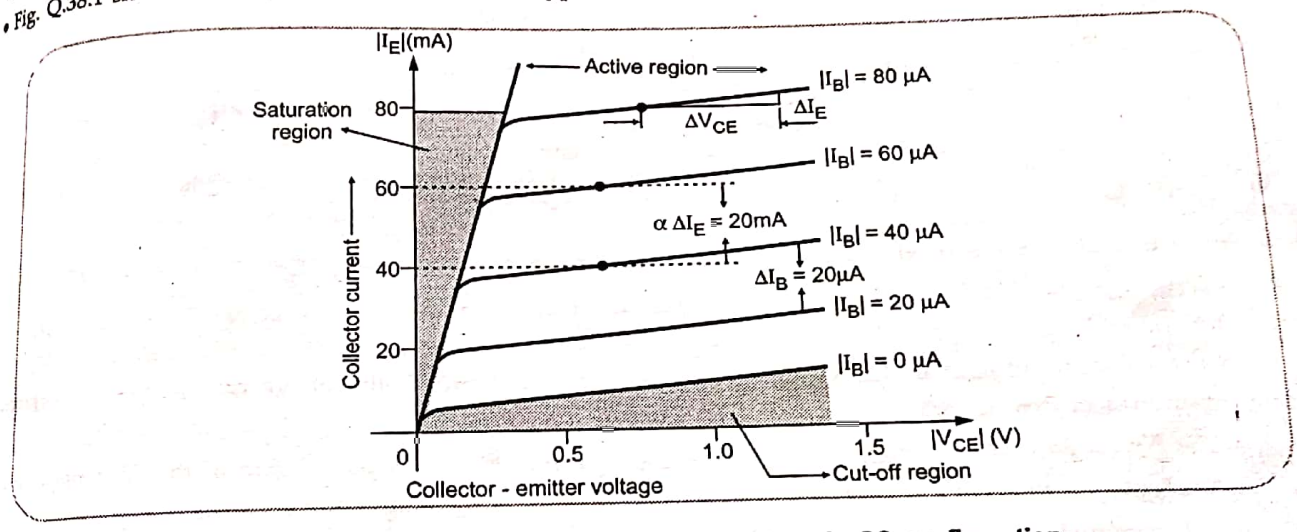

Fig. Q.38.1 Output characteristics of the transistor in CC configuration

- Since, I_C is approximately equal to I_E, the common collector output characteristics are practically similar to those of the common emitter output characteristics.

Q.39 What is the current gain of CC configuration ? ☞[JNTU : Part A]

Ans. : • The current gain of CC configuration is given by

$$\gamma = \frac{I_E}{I_B} = \frac{I_B + I_C}{I_B} = 1 + \frac{I_C}{I_B} = 1 + \beta = 1 + \frac{\alpha}{1-\alpha} = \frac{1}{1-\alpha}$$

Q.40 Explain how a BJT acts as an current amplifier. ☞ [JNTU : Sept.-17, Marks 3]

Ans. : In CC configuration, the output current is emitter current, I_E and input current which controls the output current is I_B. The output current, I_E is $1+\beta$ times input current I_B and hence in this configuration, BJT acts as an current amplifier.

Q.41 Compare CB, CE and CC transistor configurations. ☞[JNTU : Part B, Sept. - 17, April - 18, Aug. - 18, May - 19, Marks 5]

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Ans. :

Sr. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance (R_i)	Very low (20 Ω)	Low (1kΩ)	High (500 kΩ)
2.	Output resistance (R_o)	Very high (1 MΩ)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and base	Base and emitter	Base and collector
6.	Output voltage taken between	Collector and base	Collector and emitter	Emitter and collector
7.	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain (A_i)	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain (A_v)	Medium	Medium	Less than unity
10.	Applications	As a input stage of multistage amplifier	Provides both voltage and current gain greater than unity and hence it is widely used in audio signal amplification	For impedance matching

Q.42 Why CE configuration is widely used in amplifier circuits ? ☞[JNTU : Part A]

Ans. : • The common-emitter configuration is widely used amongst three transistor configurations. The main reasons for the wide-spread use of this circuit arrangement are :

- The CE configuration is the only configuration which provides both voltage gain as well as current gain greater than unity.
- The power gain is a product of voltage gain and current gain. The power gain of the CE amplifier is much greater than the power gain provided by the other two configurations.
- In a common emitter circuit, the ratio of output resistance to input resistance is small, may range from 10 Ω to 100 Ω. This makes configuration an ideal for coupling between various transistor stages.

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UNIT - V

8 Field Effect Transistor (FET)

8.1 : Introduction

Q.1 What is FET ?

☞ [JNTU : Part A]

Ans. : • The Field Effect Transistor abbreviated as FET is an another semiconductor device like a BJT which can be used as an amplifier or switch.

• Like BJT, FET is also a three terminal device;

• The three terminals of FET are named as Drain (D), Source (S) and Gate (G), as shown in the Fig. Q.1.1. Out of these three terminals gate terminal acts as a controlling terminal.

Q.2 List Important features of FET.

☞ [JNTU : Part B]

Ans. : Voltage Controlled Device

• Unipolar Device

• FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called **unipolar device.**

• Unlike BJT, thermal runaway does not occur with FET. Thus we can say that FET is **more temperature stable** as compared to the BJT.

• FET has **very high input impedance.**

• FETs **require less space** than that for BJTs, hence they are preferred in integrated circuits.

Q.3 State the types of FET.

☞ [JNTU : Part A]

Ans. : • The FETs are categorised as :

- Junction Field Effect Transistors (JFETs),
- Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

8.2 : Construction of FET

Q.4 Explain with neat sketch construction of n-channel FET.

☞ [JNTU : Aug.-18, May-19, Marks 3]

OR Draw symbols of n-channel JFET.

☞ [JNTU : Part B]

Ans. : • The Fig. Q.4.1 shows structure and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and at its two ends, two ohmic contacts are made which are the drain and source terminals of FET.

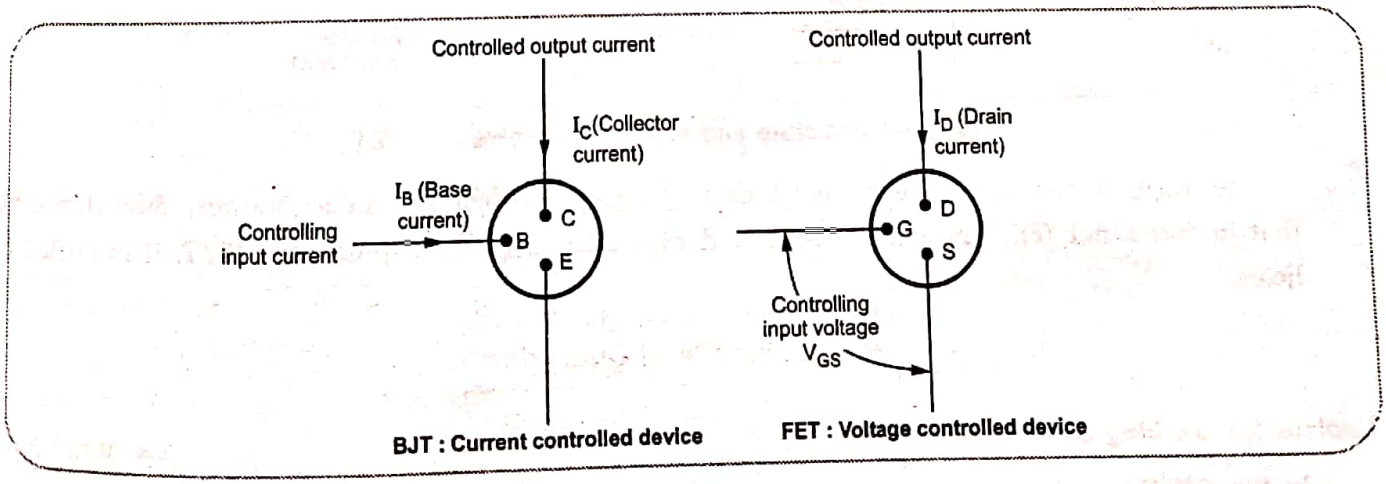

Fig. Q.1.1 Controlling element for BJT and FET

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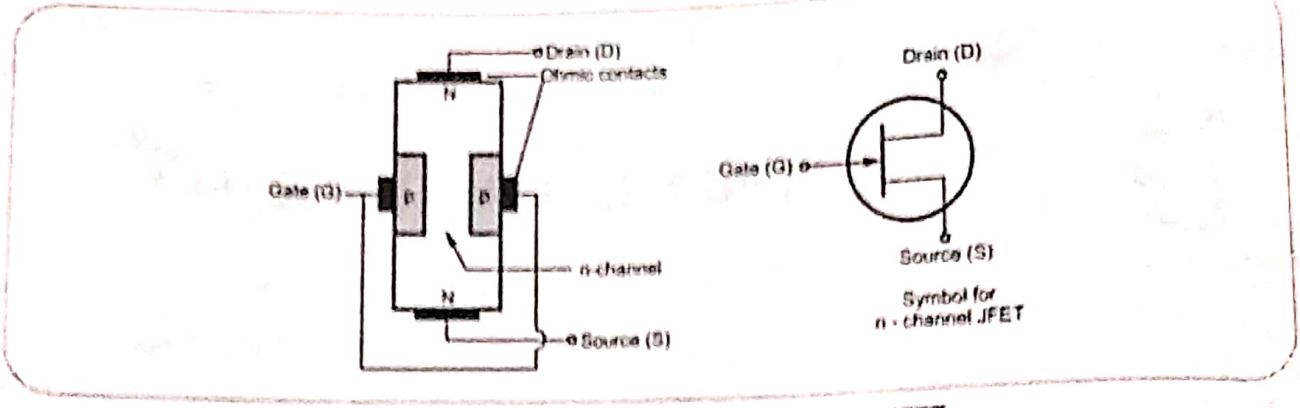

Fig. Q.4.1 Structure and symbol for n-channel JFET

- Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the **channel**. Since this channel is in the n type bar, the FET is known as **n-channel JFET.**
- The electrons enter the channel through the terminal called **source** and leave through the terminal called **drain**. The terminals taken out from heavily doped electrodes of p type material are called **gates**. Usually, these electrodes are connected together and only one terminal is taken out, which is called **gate**, as shown in the Fig. Q.4.1.

Q.5 Explain with neat sketch construction of p-channel FET. ☞ **[JNTU : Part B]**

OR Draw the symbol of n-channel and p-channel JFET. ☞ **[JNTU : April-18, Marks 2]**

Ans. : • The device could be made of p type bar with two n type gates as shown in the Fig. Q.5.1. Then this will be p-channel JFET.

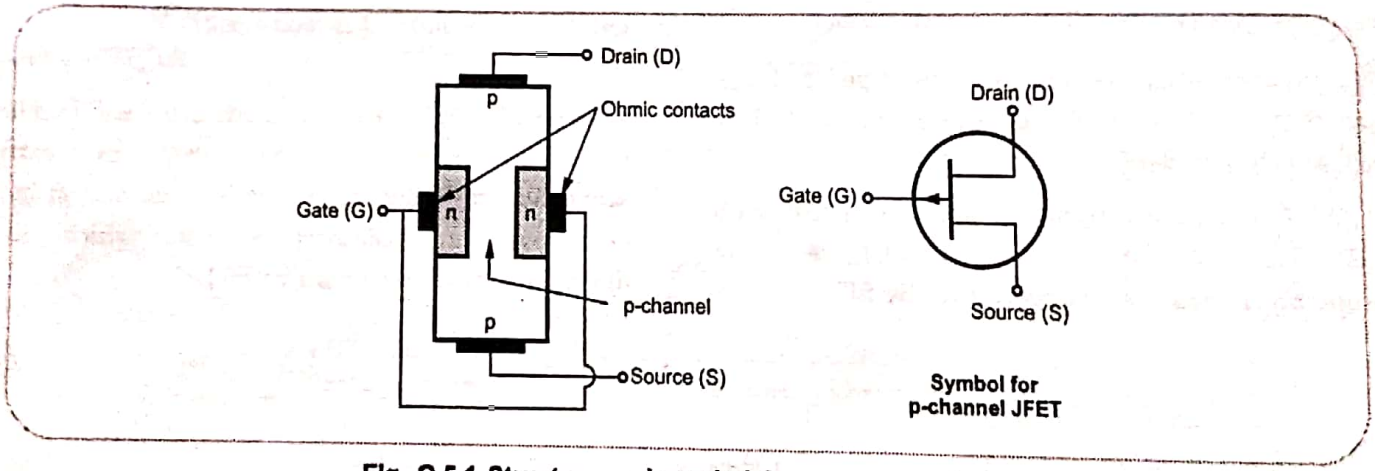

Fig. Q.5.1 Structure and symbol for p-channel JFET

- The principle of working of n-channel JFET and p-channel JFET is similar; the only difference being that in **n-channel JFET** the current is carried by electrons while in **p-channel JFET**, it is carried by holes.

8.3 : Principle of Operation

Q.6 Explain the working of n-channel FET. ☞ **[JNTU : Part B]**

OR Explain the details about the principle of operation of JFET. ☞ **[JNTU : June-17, Aug.-18, May-19, Marks 5]**

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Ans. : • When voltage is applied between the drain and source with DC supply V_{DS}, electrons flow from source to drain through the narrow channel existing between the depletion regions. This causes a drain current ID to flow from drain to source.

• When the gate is shorted to source as shown in Fig. Q.6.1 (a), there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by I_{DSS}.

• When the gate to source voltage V_{GS} is increased with negative value as shown in Fig. Q.6.1 (b), the reverse bias voltage across gate to source increases. As a result, the width of the depletion region increases. This reduces the width of the channel and thus controls the drain current I_D.

• It is observed that the channel is narrower at the drain end. This happens because amount of reverse bias is not same throughout the length of p-n junction.

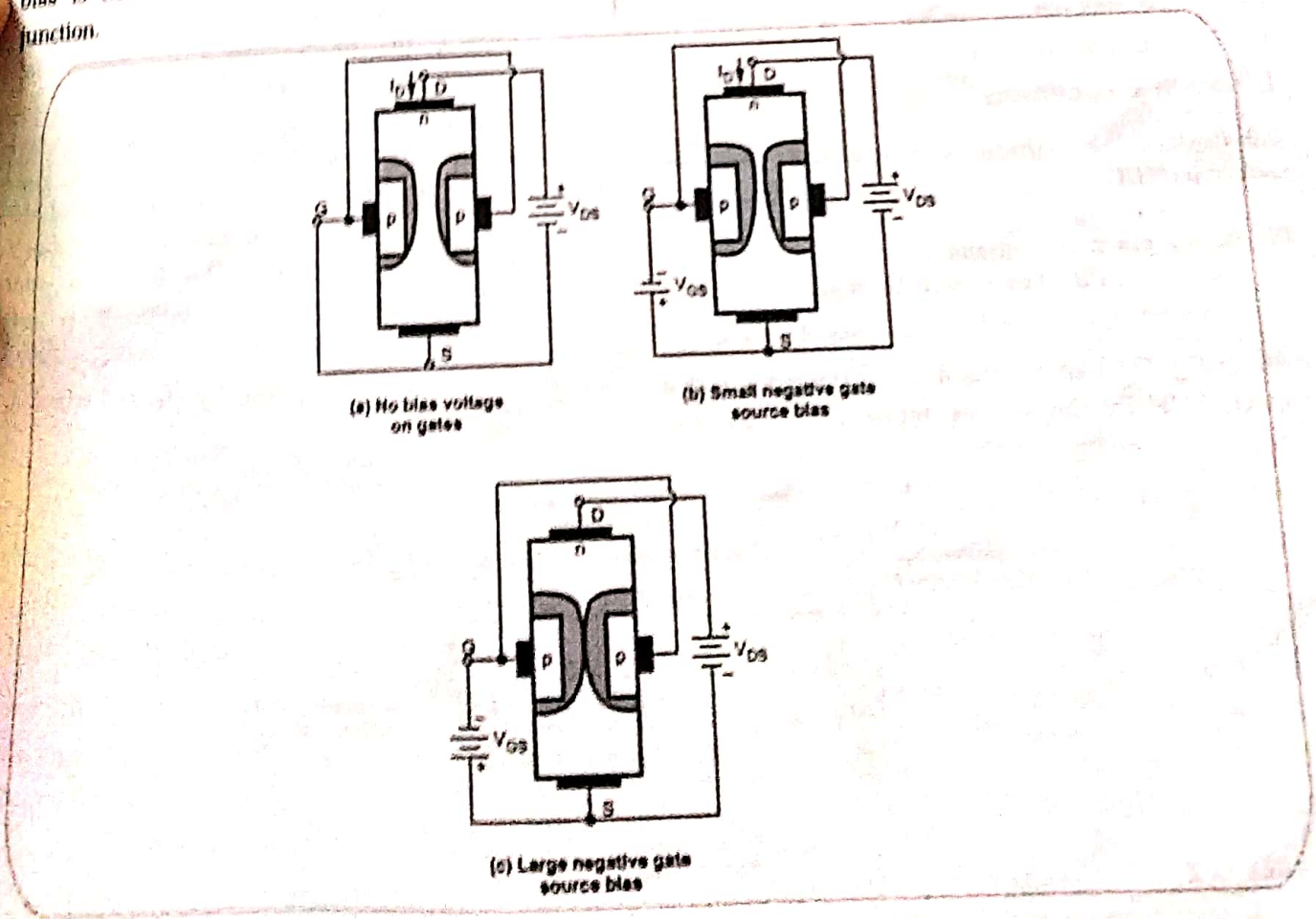
• When negative value of V_{GS} is increased further, a stage is reached at which two depletion regions touch each other leaving zero width for conducting portion of the channel as shown in the Fig. Q.6.1 (c). This will prevent any current flow from drain to source and hence cut off the drain current. The gate to source voltage that produces cut-off is known as **cut-off voltage** and it is denoted by $V_{GS(off)}$.

• From above discussion it is cleared that the gate to source voltage controls the current flowing through channel and hence FET is also called **voltage controlled current source.**

Q.7 Explain the working of p-channel FET.

[JNTU : Part B]

Ans. : • The p-channel JFET is constructed in exactly the same manner as the n-channel JFET but with reversal of the p-and n-type materials as shown in the Fig. Q.7.1.



(a) No bias voltage on gates

(b) Small negative gate source bias

(c) Large negative gate source bias

Fig. Q.6.1 The effect of gate voltage on channel- width and on drain current I_D

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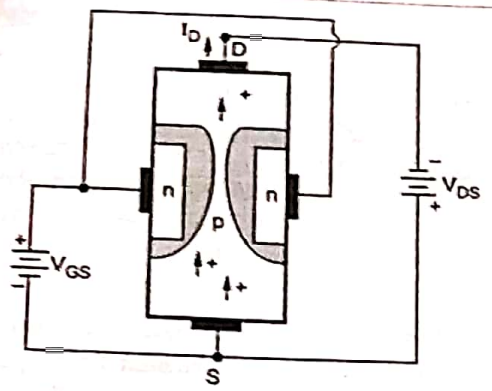

Fig. Q.7.1 p-channel FET

- All current directions and voltage polarities are reversed

For V_{GS} = 0, channel width is maximum. By increasing positive gate to source (V_{GS}) voltage, the channel width is reduced.

Q.8 List the important characteristics of JFET.

☞ [JNTU : Part A]

Ans. : The important characteristics of JFET are :

1. Drain characteristics and
2. Transfer characteristics

Q.9 Explain the drain characteristics for an n-channel FET.

OR Define pinch off voltage.

☞ [JNTU : Part B, April-18, Marks 5, Sept.-17, Aug.-18, Marks 2]

Ans. : • Fig. Q.9.1 shows the drain characteristics of a n-channel JFET. The curves represent relationship between the drain current and drain to source voltage for different values of V_{GS}.

1. **Ohmic Region :** Shown by curve OA in Fig. Q.9.1. In this region the drain current increases linearly with the increase in drain to source voltage V_{DS}. here, JFET acts as a simple resistor.
2. **Pinch-Off Voltage (V_p) :** At some value of V_{DS} (shown by point A for V_{GS} = 0), drain current I_D cannot be increased further, due to reduction in channel width. Any further increase in V_{DS} does not increase the drain current I_D. I_D approaches the constant saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called **'Pinch-Off Voltage'**, V_p. From Fig. Q.9.1 it can be observed that for more negative values of V_{GS}, the pinch-off voltage is reached at lesser values of I_D.
3. **Saturation Region (Pinch-off Region) :** This region shown by AB curve. In the saturation region, the drain current I_D remains fairly constant and does not vary with V_{DS}.
4. **Break down Region :** In this region the drain current increases rapidly as the drain to source voltage increases. This happens because of break down of gate to source junction due to avalanche breakdown. The drain to source voltage corresponding to point B is called breakdown voltage VBR.
5. **Relation of $V_{GS\,(off)}$ and V_p :** I_D is 0 when $V_{GS} = -V_p$.

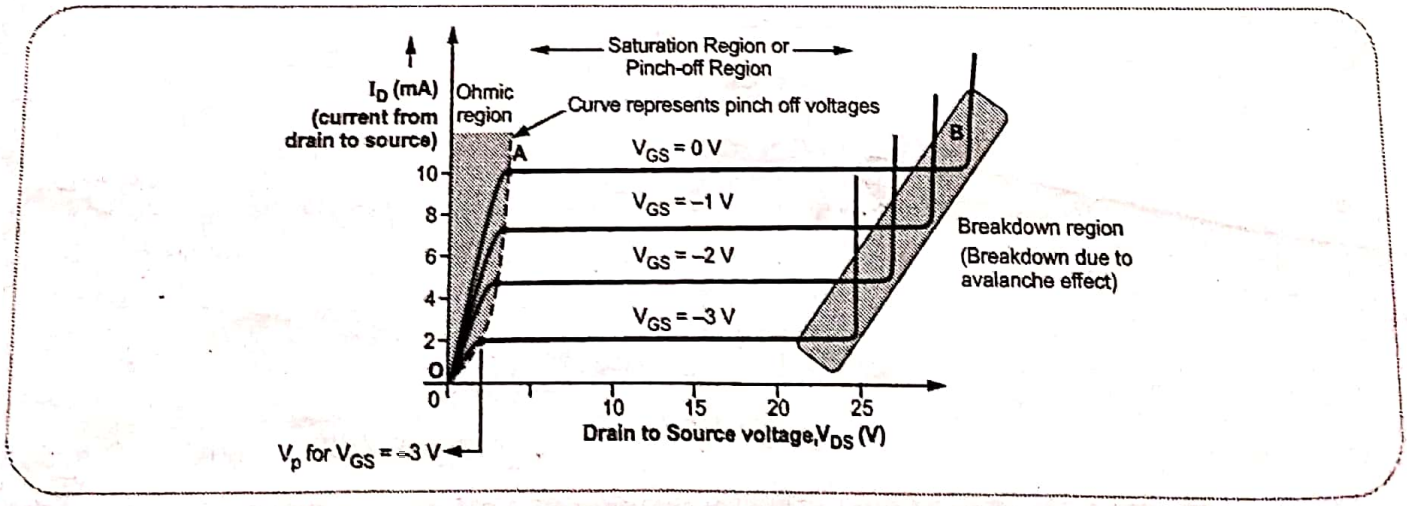

Fig. Q.9.1 Drain V-I characteristics of n-channel JFET

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Q.10 Explain the drain characteristics for p-channel FET. ☞ [JNTU : Part B]

Ans. : • In a p-channel JFET the source is positive with respect to the drain. Here the source is the source of holes which flow through the channel to the drain. The pinch-off is achieved by making the source to gate voltage, V_{SG} negative (i.e. V_{GS} positive) there by reverse biasing the p-n junction diode formed by the channel and the gate.

• The Fig. Q.10.1 shows the drain characteristics of p-channel JFET. Note the similarities between these characteristics and those shown for n-channel JFET in Fig. Q.9.1.

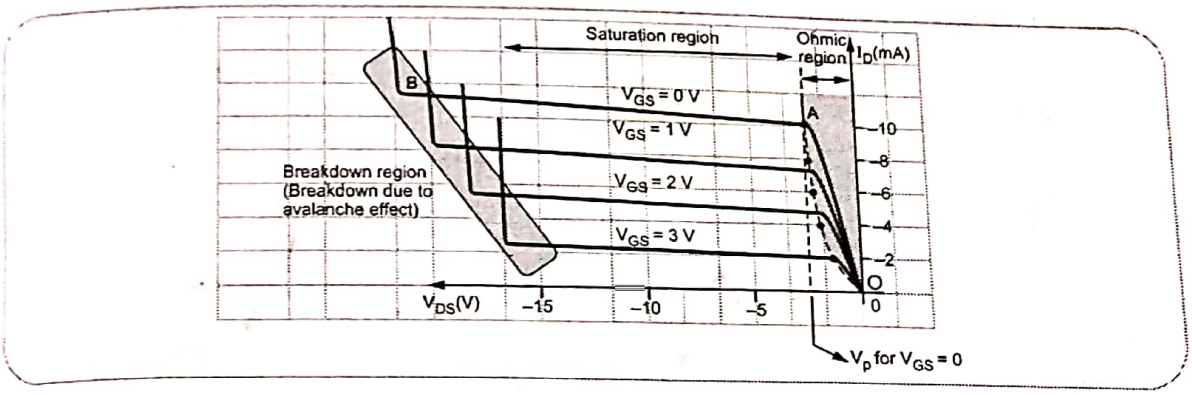

Fig. Q.10.1 Drain V-I characteristics of p-channel JFET

• The curves are identical except that voltage V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.

Q.11 Explain the transfer characteristics for n-channel JFET. ☞ [JNTU : Part B]

Ans. : Square Law Expression for I_D

• The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear as shown in the Fig. Q.11.1 This relationship is defined by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad \ldots (1)$$

• The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}. From equation we can also write,

$$V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

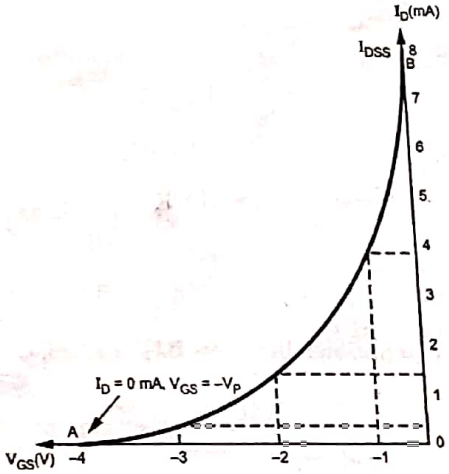

Fig. Q.11.1 Transfer characteristics of n-channel JFET

• In the equation values of I_{DSS} and V_p are constants, value of V_{GS} controls I_D.

• A point A at the bottom end of the curve on the V_{GS}-axis represents $V_{GS\,(off)}$, and point B at the top end of the curve on the I_D axis represents I_{DSS} (maximum drain current at V_{GS} =0).

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Thus, this curve shows the operating limits of a JFET. These are :

- $I_D = 0$ when $V_{GS} = V_{GS(off)}$
- $I_D = I_{DSS}$ when $V_{GS} = 0$

Q.12 Explain the transfer characteristics for p-channel JFET.

☞ [JNTU : Part B]

Ans. : The Fig. Q.12.1 shows the transfer characteristics of p-channel JFET. It is identical to transfer characteristics of n-channel JFET except that the polarities of V_{GS} and I_D are reversed.

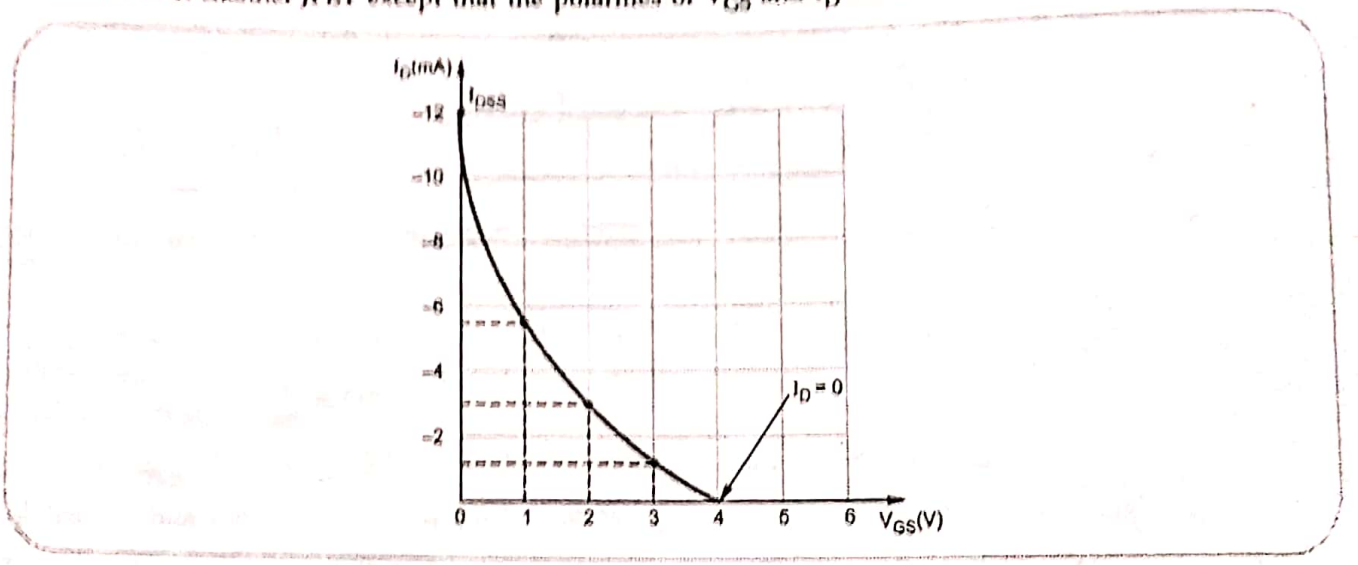

Fig. Q.12.1 Transfer characteristics of p-channel JFET

Q.13 For JFET, determine I_D, if I_{DSS} = 12 mA, V_p = – 4 V and V_{GS} = – 1.

☞ [JNTU : Part B, Dec.-18, Marks 5]

Ans. :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

$$= 12\times10^{-3}\left(1-\frac{(-1)}{(-4)}\right)^2 = 6.75 \text{ mA}$$

8.4 : Comparison of BJT and FET

Q.14 Give comparison between BJT and FET.

☞ [JNTU : Part B, April-18, June-17, Aug.-18, May-19, Sept-17, Marks 5]

Ans. :

Sr. No.	Parameter	BJT	FET
1.	Control element	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2.	Device type	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3.	Types	n-p-n and p-n-p	n-channel and p-channel.

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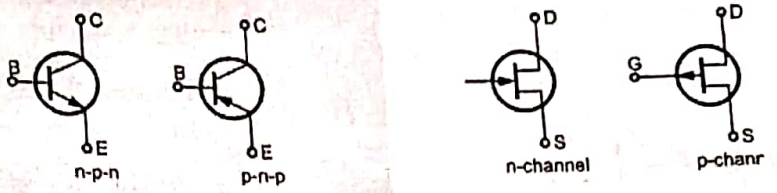
4.	Symbols		
5.	Configurations	CE, CB, CC	CS, CG, CD
6.	Input resistance	Less compare to JFET.	High compare to BJT.
7.	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in Integrated - Circuits (IC).
8.	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9.	Thermal stability	Less	More
10.	Thermal runaway	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11.	Relation between input and output	Linear	Non-linear
12.	Ratio of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13.	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14.	Gain bandwidth product	High	Low

8.5 : Biasing of FET

Q.15 Comment on FET biasing in ohmic region and active region. ☞ [JNTU : Part A]

Ans. : • The JFET can be biased in the ohmic or in the active region.

- When biased in the ohmic region, the JFET in equivalent to a resistance.
- When biased in the active region, the JFET is equivalent to a current source.

Q.16 Explain the gate bias circuit used to bias FET in ohmic region. ☞ [JNTU : Part B]

Ans. : • Fig. Q.16.1 shows the gate bias circuit for the n-channel JFET. This is the simplest biasing arrangement. (See Fig. Q.16.1 on next page).

- To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.
- For the d.c. analysis coupling capacitors are open circuits. The current through R_G is I_G which is zero.

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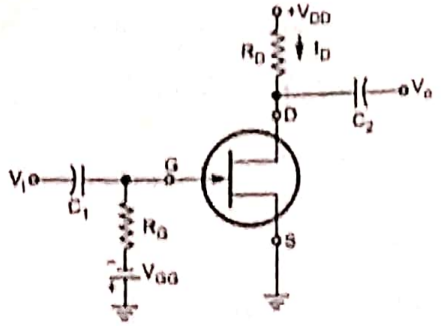

Fig. Q.16.1 Gate bias circuit for n-channel circuit

- This permits R_G to replace by short circuit equivalent, simplifying the gate bias circuit as shown in the Fig. Q.16.2

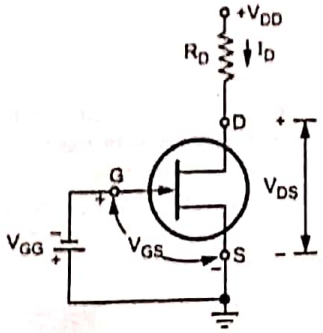

Fig. Q.16.2 Simplified gate bias circuit

Step 1 : Calculate V_{GS}

- We know for d.c. analysis $I_G = 0$ A and applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$\therefore \quad V_{GS} = -V_{GG} \qquad \ldots (Q.16.1)$$

- Since V_{GG} is a fixed d.c. supply, the voltage V_{GS} is fixed in magnitude and hence the name gate bias circuit.

Step 2 : Calculate I_{DQ}

- The drain current I_D can be calculated using equation.

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Step 3 : Calculate V_{DS}

- The drain to source voltage of drain circuit can be determined by applying KVL.

$$V_{DD} - I_D R_D - V_{DSQ} = 0$$

$$\therefore \quad V_{DSQ} = V_{DD} - I_D R_D \qquad \ldots (Q.16.2)$$

- The main drawback of gate bias circuit of FET is that it requires two power supplies.

To ensure that a JFET is biased in the ohmic region, all we have to use $V_{GS} = 0$ and $I_{D(sat)} << I_{DSS}$.

Q.17 For the circuit shown in the Fig. Q.17.1 Calculate : a) V_{GSQ}, b) I_{DQ}, c) V_{DSQ}, d) V_D [JNTU : Part B]

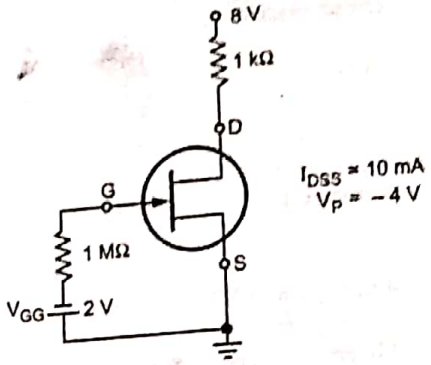

Fig. Q.17.1

Ans. :

a) $V_{GSQ} = -V_{GG} = -2$ V $\quad \because I_G = 0$ and $I_G R_G = 0$

b) $$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{-2\text{ V}}{-4\text{ V}}\right)^2$$

$$= 10 \times 10^{-3}\,(1 - 0.5)^2 = 10 \times 10^{-3}\,(0.25)$$

$$= \mathbf{2.5\ mA}$$

c) $$V_{DSQ} = V_{DD} - I_{DQ} R_D$$

$$= 8\text{ V} - 2.5 \times 10^{-3}\,(1 \times 10^3) = \mathbf{5.5\ V}$$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = \mathbf{5.5\ V}$

Q.18 Calculate the drain voltage for gate bias circuit with $R_D = 10$ kΩ. Assume that the JFET is based in the ohmic region. Assume $I_{DSS} = 10$ mA, $V_p = 4$ V and $V_{DD} = 10$ V. [JNTU : Part B]

Ans. : In the ohmic region, we can replace JFET by a resistance R_{DS}, as shown in the Fig. Q.18.1.

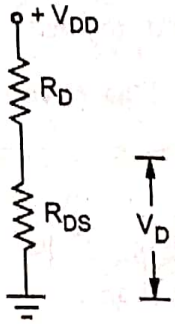

Fig. Q.18.1 JFET equivalent circuit when biased in the ohmic region

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$$R_{DS} = \frac{V_P}{I_{DSS}} = \frac{4}{10\text{ mA}} = 400\ \Omega$$

$$V_D = \frac{R_{DS}}{R_{DS} + R_D} V_{DD}$$

$$= \frac{400}{400 + 10\text{K}} \times 10 = 0.385\text{ V}$$

Q.19 Draw and explain the self bias circuit for biasing FET in active region.

[JNTU : Part B]

Ans. : • JFET must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. Q.19.1.

- The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V.
- R_G is necessary only to isolate an a.c. signal from ground in amplifier applications.
- The voltage drop across resistor, R_S makes gate source junction reverse biased.

DC Analysis :

Step 1 : Obtain expression for V_{GS}

For the n-channel FET in Fig. Q.19.1 (a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

For the p-channel FET in Fig. Q.19.1 (b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = -I_S R_S = -I_D R_S$. The gate to source voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = +I_D R_S$$

In the following D.C. analysis, the n-channel JFET shown in Fig. Q.19.1 (a) is used to for illustration. For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig. Q.19.2.

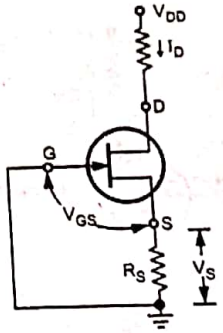
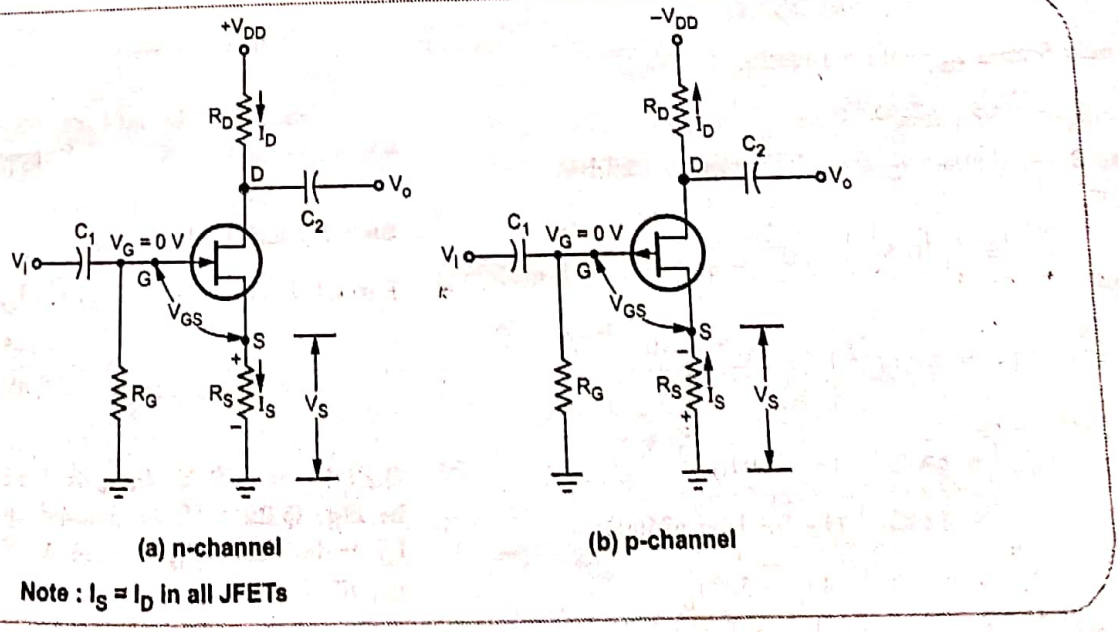


Fig. Q.18.2 Simplified self bias circuit for dc analysis



(a) n-channel **(b) p-channel**

Note : $I_S = I_D$ in all JFETs

Fig. Q.19.1 Self bias circuits for JFET

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Step 2 : Calculate I_{DQ}

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1-\frac{-I_D R_S}{V_p}\right)^2 = I_{DSS}\left(1+\frac{I_D R_S}{V_p}\right)^2$$

... (Q.19.1)

Step 3 : Calculate V_{DS}

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D$$

$$= V_{DD} - I_D(R_S + R_D)$$

Q.20 For the circuit shown in Fig. Q.20.1. Calculate V_{GSQ}, I_{DQ}, V_{DS}, V_S and V_D.

☞ [JNTU : Part B]

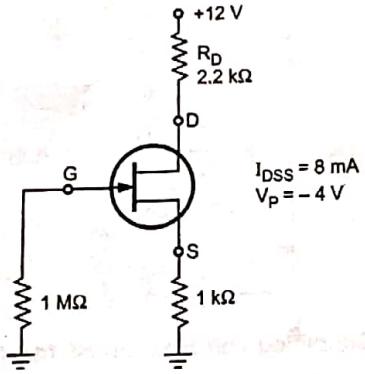

Fig. Q.20.1

Ans. : Step 1 : Obtain expression for V_{GS}

$$V_{GS} = -I_D R_S$$

Step 2 : Calculate I_D and Values of V_{GS} and V_S.

$$I_D = I_{DSS}\left(1+\frac{I_D R_S}{V_p}\right)^2$$

$$\therefore I_D = 8\times10^{-3}\left(1+\frac{I_D\times1\times10^3}{-4}\right)^2$$

$$= 8\times10^{-3}(1-250\,I_D)^2$$

$$= 8\times10^{-3}(1-500\,I_D+62500\,I_D^2)$$

$$I_D = 8\times10^{-3} - 4\,I_D + 500\,I_D^2$$

$$\therefore 500\,I_D^2 - 5\,I_D + 8\times10^{-3} = 0$$

Solving quadratic equation using formula $\frac{-b\pm\sqrt{b^2-4ac}}{2a}$ we have,

$$= \frac{+5\pm\sqrt{(-5^2)-4(500)(8\times10^{-3})}}{2\times(500)}$$

$$= \frac{+5\pm\sqrt{25-16}}{1000} = \frac{+5\pm\sqrt{9}}{1000} = \frac{+5\pm3}{1000} = 8 \text{ mA or } 2 \text{ mA}$$

I_{DQ} cannot have value 8 mA because maximum value of I_D, I_{DSS} is given as 8 mA at $V_{GS} = 0$ and hence I_{DQ} is taken as **2 mA.**

$$\therefore V_{GSQ} = -I_D R_S = -2\times10^{-3}\times1\times10^3 = -2 \text{ V}$$

$$V_S = I_D R_S = 2\times10^{-3}\times1\times10^3 = 2 \text{ V}$$

Step 3 : Calculate V_{DS}

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 12 - 2\times10^{-3}(2.2\times10^3 + 1\times10^3)$$

$$= 12 - 6.4 = 5.6 \text{ V}$$

Step 4 : Calculate V_D

$$V_D = V_{DS} + V_S = 5.6 + 2 = 7.6 \text{ V}$$

Q.21 Calculate the value of feedback resistor (R_s) required to self bias an n-channel JFET with I_{DSS} = 40 mA, V_P = – 10 and V_{GSQ} = – 5 V.

☞ [JNTU : Part B]

Ans. :

Step 1 : Calculate I_{DQ}

$$I_{DQ} = I_{DSS}\left[1-\frac{V_{GSQ}}{V_p}\right]^2$$

$$= 40\times10^{-3}\left[1-\frac{(-5)}{(-10)}\right]^2 = 10 \text{ mA}$$

Step 2 : Calculate R_S

For self bias circuit : $V_{GSQ} = -I_{DQ} R_S$

$$\therefore R_s = \frac{-V_{GSQ}}{I_{DQ}} = \frac{-(-5)}{10 \text{ mA}} = 500\ \Omega$$

Q.22 V_p = – 2 V, I_{DSS} = 1.65 mA for the circuit in Fig. Q.22.1. It is desired to bias the circuit at I_D = 0.8 mA, V_{DD} = 24 V. Calculate i) V_{GS} ii) g_m iii) R_S.

☞ [JNTU : Part B]

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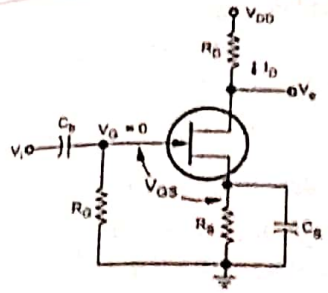

Fig. Q.22.1

Ans. : Step 1 : Calculate V_{GS}

We have $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$

$$\therefore \quad V_{GS} = V_P\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$= -2\left(1-\sqrt{\frac{0.8\times10^{-3}}{1.65\times10^{-3}}}\right) = -0.6074 \text{ V}$$

Step 2 : Calculate g_m

$$g_{mo} = \frac{-2I_{DSS}}{V_p} = \frac{-2\times1.65}{-2} = 1.65 \text{ mS}$$

$$g_m = g_{mo}\left[1-\frac{V_{GS}}{V_P}\right] = 1.65\left(1-\frac{0.6074}{2}\right)\times10^{-3}$$

$$= 1.65\times10^{-3}\times0.6963 = 1.15 \text{ mS}$$

Step 3 : Calculate R_S

$$0 = V_{GS} + I_D R_S$$

$$\therefore \quad R_S = -\frac{V_{GS}}{I_D} = -\left(\frac{0.6074}{0.8 \text{ mA}}\right) = 759.25\ \Omega$$

Q.23 The FET shown in Fig. Q.23.1 has $|I_{DSS}| = 12$ mA and $|V_p| = 5$ V. Calculate the quiescent values of i) I_D ii) V_{DS} iii) V_{GS}.

[JNTU : Part B]

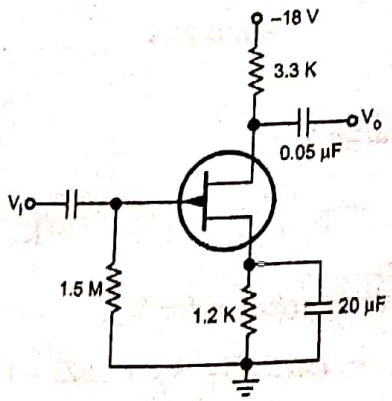

Fig. Q.23.1

Ans. : Fig. Q.23.2 shows simplified circuit for d.c. analysis

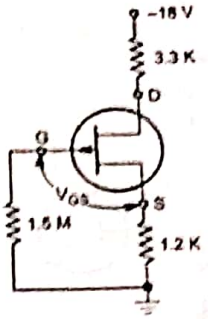

Fig. Q.23.2

Step 1 : Obtain expression for V_{GS}

Applying KVL to the input circuit we get,

$$V_{GS} - I_D R_S = 0$$

$$\therefore \quad V_{GS} = I_D R_S$$

Step 2 : Calculate I_D

We have, $I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$

Substituting value of V_{GS} in above equation and solving for I_D we get,

$$I_D = 2.33 \text{ mA or } 7.45 \text{ mA}$$

We calculate V_{DS} using $I_D = 7.45$ mA

$$V_{DS} = V_{DD} - [-I_D (R_S + R_D)]$$

$$= -18 - [-7.45\ (1.2\times10^3 + 3.3\times10^3)]$$

$$= -18 + 33.525 = 15.525 \text{ V}$$

Practically, value of V_{DS} for p-channel FET should be negative, hence value of $I_D = 7.45$ mA is invalid.

$$\therefore \quad I_D = 2.33 \text{ mA}$$

Step 3 : Calculate V_{DS} and V_{GS}.

Now calculating V_{DS} taking $I_D = 2.33$ mA

$$V_{DS} = V_{DD} - [-I_D (R_S + R_D)]$$

$$= -18 - [-2.33\times10^{-3}(1.2\times10^3 + 3.3\times10^3)]$$

$$= -18 + 10.485 = -7.515 \text{ V}$$

$$V_{GS} = I_D R_S = 2.33\times10^{-3}\times1.2\times10^3$$

$$= 2.796 \text{ V}$$

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Q.24 Draw and explain the voltage divider bias circuit for biasing FET in active region.

☞ [JNTU : Part B]

Ans. : • The Fig. Q.24.1 shows n-channel JFET with voltage divider bias.

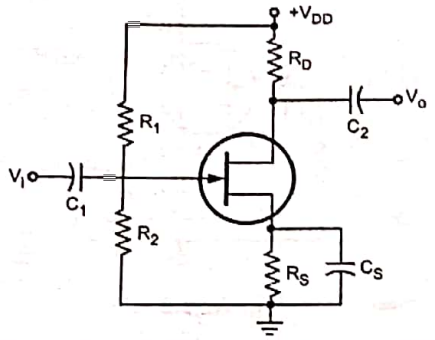

Fig. Q.24.1 Voltage divider bias for n-channel JFET

- The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.
- The source voltage is,

$$V_S = I_D R_S$$

- The gate voltage is set by resistors R_1 and R_2.
- Coupling capacitors C_1 and C_2 and source resistor bypass capacitor C_S are assumed to be open circuit for DC analysis.

Step 1 : Calculate V_G

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} \qquad \because I_G = 0$$

Step 2 : Obtain expression for V_{GS}

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - I_D R_S = 0$$

$$\therefore \quad V_{GS} = V_G - I_D R_S \qquad \ldots (Q.24.1)$$

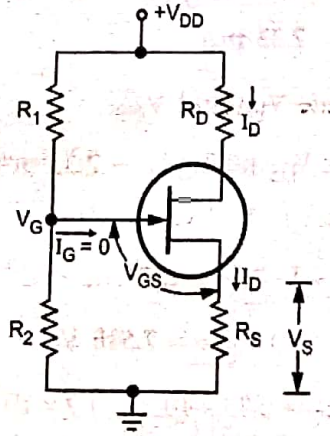

Fig. Q.24.2 Simplified voltage divider circuit for d.c. analysis

Step 3 : Calculate I_{DQ}

The I_{DQ} can be calculated using equation :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Step 4 : Calculate V_{DS} and V_{GS}

Applying KVL to the output circuit we get,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\therefore \quad V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S)$$

$$\ldots (Q.24.2)$$

The Q point of a JFET amplifier using the voltage divider bias is given by :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

$$V_{GSQ} = V_G - I_D R_S$$

Q.25 Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS} and V_{DG} for the network of Fig. Q.25.1.

☞ [JNTU : Part B]

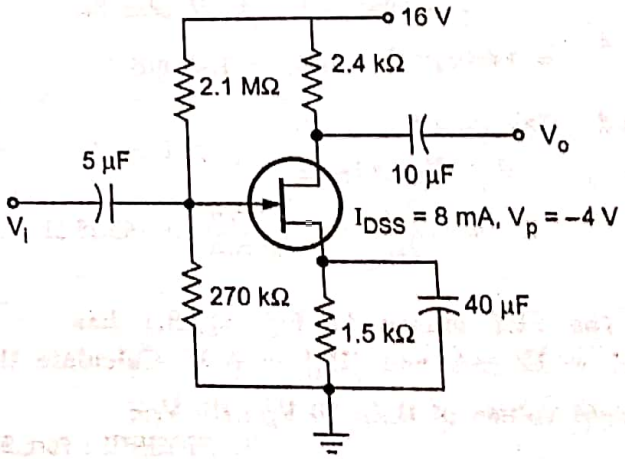

Fig. Q.25.1

Ans. :

Step 1 : Calculate V_G

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{16 \times 270\,K}{2.1\,M + 270\,K} = 1.823\ V$$

Step 2 : Obtain expression for V_{GS}

$$\therefore \quad V_{GS} = 1.823 - I_D R_S = 1.823 - 1.5 \times 10^3\, I_D$$

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Step 3 : Calculate I_D

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 8\times10^{-3}\left(1-\frac{(1.823-I_D\times1.5\times10^3)}{-4}\right)^2$$

$$= 8\times10^{-3}(1-|(-0.456+375\,I_D)|)^2 = 8\times10^{-3}(1.456-375\,I_D)^2$$

$$= 8\times10^{-3}\left(2.12-1092\,I_D+140625\,I_D^2\right)$$

$$I_D = 0.01696 - 8.736\,I_D + 1125\,I_D^2$$

$$1125\,I_D^2 - 9.736\,I_D + 0.01696 = 0$$

Solving quadratic equation using formula $\frac{-b\pm\sqrt{b^2-4ac}}{2a}$ we get,

$$= \frac{-(-9.736)\pm\sqrt{(-9.736)^2-4\times1125\times0.01696}}{2\times1125} = \frac{9.736\pm4.2976}{2\times1125}$$

$$= 6.237 \text{ mA} \quad \text{or} \quad 2.417 \text{ mA}$$

If we calculate value of V_{DS} taking I_D = 6.237 mA we get,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 16 - 6.237\times10^{-3}(2.4\text{ K}+1.5\text{ K}) = -8.3243 \text{ V}$$

Practically, the value of V_{DS} must be positive, hence

I_D = 6.237 mA is invalid.

$\therefore$ I_D = 2.417 mA

Step 4 : Calculate V_{DS}, V_{GS}, V_S, V_D and V_{DG}.

$\therefore$ $V_{DS} = V_{DD} - I_D(R_D + R_S) = 16 - 2.417\times10^{-3}(2.4\text{ K}+1.5\text{ K}) = 6.5737 \text{ V}$

$V_{GS} = 1.823 - I_D R_S = 1.823 - (2.417\times10^{-3}\times1.5\times10^3) = -1.8025 \text{ V}$

$V_S = I_D R_S = 2.417\times10^{-3}\times1.5\times10^3 = 3.6255 \text{ V}$

$V_D = V_{DD} - I_D R_D = 16 - (2.417\times10^{-3}\times2.4\times10^3) = 10.2 \text{ V}$

$V_{DG} = V_D - V_G = 10.2 - 1.823 = 8.377 \text{ V}$

Q.28 For the circuit shown in Fig. Q.25.1, the FET has V_p = 4 V, I_{DSS} = 4 mA Calculate i) I_{DSQ} ii) V_{GSQ} iii) V_{DSQ} ☞ [JNTU : Part B]

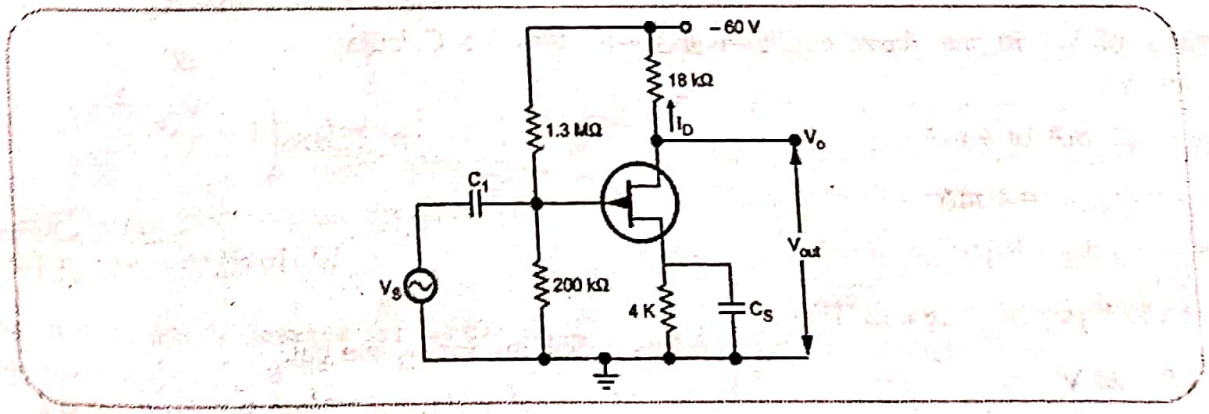

Fig. Q.26.1

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Ans. : Simplified circuit for d.c. analysis is shown in Fig. Q.26.2.

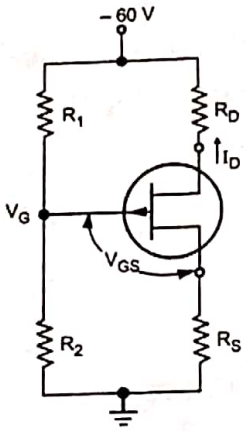

Fig. Q.26.2

Step 1 :

Calculate V_G

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{200\times10^3 \times(-60)}{1.3\times10^6 + 200\times10^3} = -8 \text{ V}$$

Step 2 : Obtain expression for V_{GS}

Applying KVL to input circuit we get,

$$V_G - V_{GS} + I_D R_S = 0$$

$$\therefore \quad V_{GS} = V_G + I_D R_S$$

$$V_{GS} = V_G + I_D R_S$$

$$= -8 + I_D R_S$$

Step 3 : Calculate I_D

We have, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in the above equation and solving for I_D we get,

$$I_D = 2.25 \text{ mA or } 4 \text{ mA}$$

We calculate V_{DS} using $I_D = 4$ mA,

$$V_{DS} = V_{DD} - (-I_D (R_S + R_D))$$

$$= -60 + 4\times10^{-3}(4\times10^3 + 18\times10^3)$$

$$= -60 + 88 = 28 \text{ V}$$

Practically, value of V_{DS} for p-channel FET should be negative, hence value of $I_D = 4$ mA is invalid.

$$\therefore \quad I_D = 2.25 \text{ mA}$$

Step 4 : Calculate V_{DS} and V_{GS}.

Now calculating V_{DS} taking $I_D = 2.25$ mA,

$$V_{DS} = -60 - (-2.25\times10^{-3}(4\times10^3 + 18\times10^3))$$

$$= -60 - 49.5 = -10.5 \text{ V}$$

$$V_{GS} = -8 + I_D R_S = -8 + 2.25\times10^{-3}(4\times10^3)$$

$$= -8 + 9 = 1 \text{ V}$$

Q.27 For the network shown in Fig. Q.27.1, determine I_D, V_{GS}, V_G, V_D, V_S and V_{DS}. **[JNTU : Part B]**

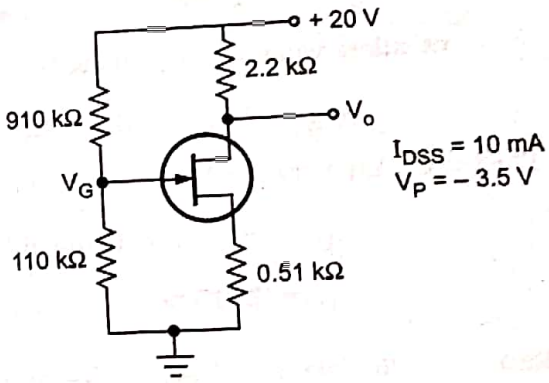

Fig. Q.27.1

Ans. :

Step 1 : Calculate V_G

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{20 \times 110}{910 + 110} = 2.157 \text{ V}$$

Step 2 : Obtain expression of V_{GS}

$$\therefore \quad V_{GS} = V_G - V_S = 2.157 - I_D R_S$$

$$= 2.157 - 510\, I_D$$

Step 3 : Calculate I_D

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10\times10^{-3}\left(1 - \frac{(2.157 - 510\, I_D)}{-3.5}\right)^2$$

Solving for I_D we get,

$$I_D = 20.98 \text{ mA or } 5.863 \text{ mA}$$

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For I_D = 20.98 mA

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 20 - 20.98\ (2.2 + 0.51) = -36.85$ V

Practically, the value of V_{DS} must be positive, hence I_D = 20.98 mA is invalid.

I_D = 5.863 mA

∴ **Step 4 :** Calculate V_{GS}, V_D, V_S and V_{DS}

$V_{GS} = 2.157 - I_D R_S$

$= 2.157 - 5.863 \times 0.51 = -0.833$ V

$V_D = V_{DD} - I_D R_D$

$= 20 - 5.863 \times 2.2 = 7.1$ V

$V_{DS} V_S = I_D R_S = 5.863 \times 0.51 = 2.99$ V

$V_{DS} = V_D - V_S = 7.1 - 2.99 = 4.11$ V

8.6 : JFET Parameters

Q.28 List the important parameters of JFET.
☞ [JNTU : Part A]

Ans. : • The important parametres of JFET are as follows :

- Input resistance
- DC drain resistance
- Dynamic (AC) Drain resistance (r_d)
- Transconductance (g_m)
- Amplification factor (μ)

Q.29 What is the input resistance of JFET ?
☞ [JNTU : Part A]

Ans. : • The input junction of JFET (gate - source junction) is reverse-biased and hence its input resistance is very high. The input resistance of JFET can be determined from a value of the gate reverse current, I_{GSS} at a certain gate-to-source voltage.

It is given by,

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

• Since I_{GSS} increases with temperature, input resistance decreases with temperature.

Q.30 Calculate the input resistance of JFET if I_{GSS} = – 2 nA when V_{GS} = – 15 V.
☞ [JNTU : Part A]

Ans. : $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{15}{2 \times 10^{-9}} = 7500$ MΩ

Q.31 What is DC drain resistance ?
☞ [JNTU : Part A]

Ans. : • The DC drain resistance is the resistance between drain and source terminals for the corresponding value of drain current, I_D and V_{DS}. It is denoted by R_D and mathematically given by,

$$R_D = \frac{V_{DS}}{I_D}$$

• Its value is few hundred kΩ.

Q.32 What is AC (Dynamic) drain resistance ?
☞ [JNTU : Part A]

Ans. : • The drain resistance r_d is the a.c. resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain characteristic in the saturation region.

• It is given by,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ \text{constant}}$$

Q.33 What is JFET forward transconductance ?

OR Derive the expression for forward transconductance.
☞ [JNTU : Part B]

Ans. : • The forward transconductance, g_m, is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant.

• The forward transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\ \text{constant}}$$

• It is the slope of the transfer characteristic.

• The forward transconductance g_m is also called **mutual conductance.** The practical unit for g_m is mS (millisiemen) or mA/V.

• We can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following equation

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$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] \quad \ldots (Q.33.1)$$

where g_{mo} is the value of g_m for $V_{GS} = 0$, and is given by,

$$g_{mo} = \frac{-2 I_{DSS}}{V_p} \quad \ldots (Q.33.2)$$

- This can be proved as given below. We know that,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \quad \ldots (Q.33.3)$$

- Differentiating this equation with respect to V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2 I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$= g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right]$$

where $g_{mo} = \frac{-2 I_{DSS}}{V_p}$

Q.34 For JFET, if I_{DSS} = 20 mA, $V_{GS(off)}$ = – 5 V, and g_{mo} = 4 mS or mA/V. Determine the transconductance for V_{GS} = – 4 V, and find I_D at this point.

☞ [JNTU : Part B]

Ans. : From equation (Q.34.1) we have,

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] = 4 \times 10^{-3}\left[1 - \frac{-4\,V}{-5\,V}\right]$$

$$= 4 \times 10^{-3} \times 0.2 = 0.8\ mS$$

We have, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$

$$= 20 \times 10^{-3}\left[1 - \frac{-4\,V}{-5\,V}\right]^2$$

$$= 20 \times 10^{-3} \times 0.04 = 0.8\ mA$$

Q.35 What is amplification factor of JFET ?

☞ [JNTU : Part A, Sept.-17, Marks 2]

Ans. : • The amplification factor, denoted by μ is defined as,

Amplification factor, $\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D \text{ constant}}$

$$\therefore \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_m$$

- Since the parameter μ is the ratio of two similar quantities viz. ratio of two voltages; μ is unitless.

8.7 : JFET Amplification and Switching

Q.36 Explain the operation of JFET as a switch.

☞ [JNTU : Part B]

Ans. : • For n-channel JFET when V_{GS} is sufficiently negative, I_D is reduced to 0. This represents OFF condition of switch. At this condition (cut-off) the value of V_{GS} is designated as V_{GS} (off). The ON resistance of JFET range from about 100 Ω to 100 K. When JFET is heavily driven i.e. when V_{GS} is more positive in case of n-channel JFET $r_{d\ (ON)}$ is minimum (about 100 Ω). This represents ON condition of switch. The bipolar transistor has the advantage over the field effect device in that ON-resistance is usually only a few ohms, and hence is much smaller than ON-resistance of JFET.

- In short, we can say that by making $V_{GS} = V_{GS(off)}$ we can open the switch and by making V_{GS} sufficiently positive we can close the switch.
- Fig. Q.36.1 shows JFET as an analog switch V_{GS} is either 0 V, which causes the JFET to conduct, or V_G, a negative voltage that cuts the JFET off. The output voltage of the switch, v_o is the drain to source voltage, which will be either v_d (when JFET is cut-off) or close to 0 (when the JFET is conducting).

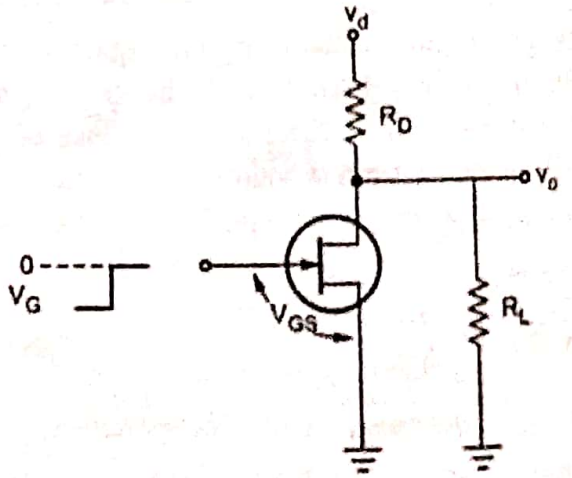

Fig. Q.36.1

Q.37 Write a note on JFET as an amplifier.

☞ [JNTU : Part B]

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Ans. : • Let us discuss the use of the JFET as an amplifier by considering the common-source circuit, shown in the Fig. Q.37.1.

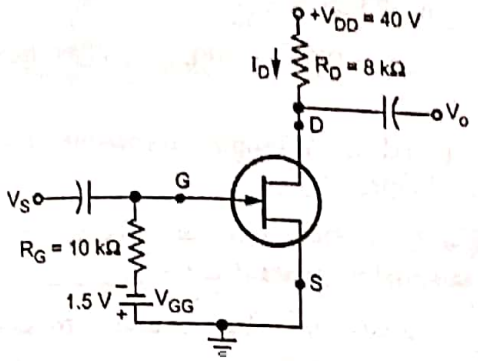

Fig. Q.37.1 Common source circuit

- The voltage V_{GG} provides the necessary reverse-bias between gate and source of the JFET. The signal to be amplified is V_s. The V-I characteristics of the JFET is as shown in Fig. Q.37.1.
- On the output characteristics, a load line corresponding to $V_{DD} = 40$ V and $R_D = 8$ kΩ is constructed. The transistor is biased at point Q and results in $V_{DSQ} = 20$ V and $I_{DQ} = 2.70$ mA.
- Assuming that the signal voltage V_s is a sinusoid of peak voltage $V_m = 0.5$ V, this signal is superimposed on the quiescent level. The instantaneous gate-to source voltage is

$$V_{gs} = V_s - V_{GG}$$

- Both quantities, I_D and V_{DS}, can be considered as sinusoids superimposed on the d.c. values.

Then $$V_{GS} = -V_{GG} + V_{gs} = -1.5 + 0.5 \sin \omega t$$

$$I_D = I_{DQ} + i_d = 2.70 + 0.5 \sin \omega t \text{ mA}$$

$$V_{out} = V_{DS} = V_{DSQ} + v_{ds} = 20 + 4 \sin \omega t$$

- We observe that the output signal is greater than the input signal, thus indicating amplification.
- The magnitude of the voltage gain $|A_v|$ is the ratio of the output a.c. signal amplitude [4.0 V] to the input a.c. signal amplitude [0.5 V]. Then, in this example,

$$|A_v| = \frac{4.0}{0.5} = 8$$

8.8 : JFET Advantages, Disadvantages and Applications

Q.38 List the advantages of JFET.

☞ [JNTU : Part B]

Ans. : The advantages of FET are :

1. Extremely high input impedance, typically, of 100 meg-ohms.
2. Lower noise than BJT.
3. Easier to fabricate and are particularly suitable for ICs.
4. No offset voltage such as base-to-emitter voltage in BJT. This property is very important in the applications like switch, chopper, etc.
5. Immune to radiation.
6. Better thermal stability.
7. Low input capacitance.
8. Low frequency drift.
9. Draws very low power in the digital circuitry.

Q.39 List the disadvantages of JFET.

☞ [JNTU : Part A]

Ans. : Disadvantages of FET are :

1. Poor performance at high frequency.
2. Small gain-bandwidth in comparison to the BJT.
3. Poor voltage gain.
4. Can be operated only in low power applications.

Q.40 List the applications of JFET.

☞ [JNTU : Part a]

Ans. : Applications of FET are :

- In general, like BJTs the FETs can be used in switch, digital and linear amplifier applications. Let us see specific applications of FET.
- Since JFET has high input impedance and low output impedance they are used as a buffer in measuring instruments.
- Because of low noise, they are used in RF amplifiers in FM tuners and in communication equipments.
- Since the input capacitance of FET is low, it is used in cascade amplifiers in measuring and test equipments.

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